CS8427

96 kHz Digital Audio Interface Transceiver

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF compatible transceiver
- +3V to +5V Digital Supply
- Flexible 3-wire serial digital I/O ports
- Adjustable sample rate up to 96 kHz
- Low jitter clock recovery
- Pin and microcontroller read/write access to Channel Status and User data
- Microcontroller and stand-alone modes
- Differential cable driver & receiver
- On-chip Channel Status and User data buffer memory provides block reads & writes
- OMCK System Clock Mode
- Decodes Audio CD Q sub-code

General Description

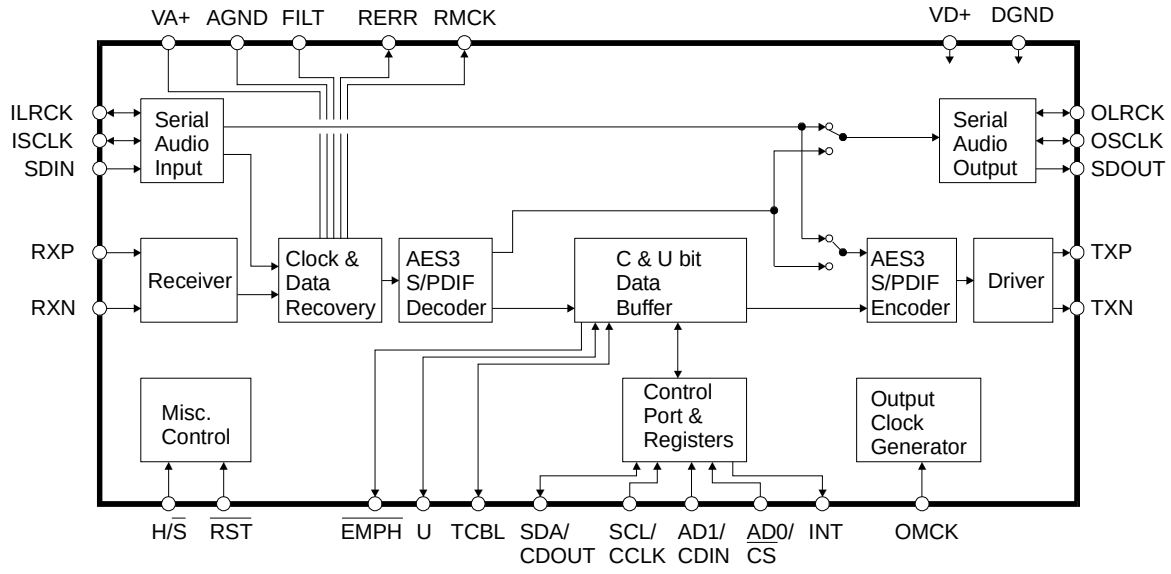
The CS8427 is a stereo digital audio transceiver with AES3 and serial digital audio inputs, AES3 and serial digital audio outputs, along with comprehensive control ability via a 4-wire microcontroller port. Channel status and user data are assembled in block sized buffers, making read/modify/write cycles easy.

A low jitter clock recovery mechanism yields a very clean recovered clock from the incoming AES3 stream.

Target applications include CD-R, DAT, MD and VTR equipment, mixing consoles, digital audio transmission equipment, high quality D/A and A/D converters, effects processors, set-top box and computer audio systems.

ORDERING INFO

CS8427-CS	28-pin SOIC, -10 to +70°C
CS8427-CZ	28-pin TSSOP, -10 to +70°C
CDB8427	Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

POWER AND THERMAL CHARACTERISTICS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		VA+	4.5	5.0	5.5	V
		VD+	2.7	3.0/5.0	5.5	V
Supply Current at 48kHz frame rate	VA+		-	TBD	TBD	mA
	VD+ = 3V		-	TBD	TBD	mA
	VD+ = 5V		-	TBD	TBD	mA
Supply Current at 96kHz frame rate	VA+		-	TBD	TBD	mA
	VD+ = 3V		-	TBD	TBD	mA
	VD+ = 5V		-	TBD	TBD	mA
Supply Current in power down	Reset high, VA+		-	TBD	-	mA
	Reset high, VD+ = 3V		-	TBD	-	mA
	Reset high, VD+ = 5V		-	TBD	-	mA
Ambient Operating Temperature	(Note 1)	T_A	-10	25	70	°C
Junction Temperature		T_J	-	-	135	°C
Junction to Ambient thermal impedance	(28 pin SOIC)	θ_{JA}	-	65	-	°C/W
	(28 pin TSSOP)		-	87	-	°C/W

Notes: 1. '-CS' and 'CZ' parts are specified to operate over -10°C to 70 °C but are tested at 25 °C only.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VD+,VA+	-	6.0	V
Input Current, Any Pin Except Supply, TXP, TXN (Note 2)	I_{in}	-	±10	mA
Input Current, TXP, TXN	I_{in}	-	±TBD	mA
Input Voltage	V_{in}	-0.3	(VD+) + 0.3	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 2. Transient currents of up to 100mA will not cause SCR latch-up.

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+ = 5V, VD+ = 3/5V ±10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage, except RXP, RXN	V_{IH}	2.0	-	(VD+) + 0.3	V
Low-Level Input Voltage, except RXP, RXN	V_{IL}	-0.3	-	0.8	V
Low-Level Output Voltage, (Io=-20uA), except TXP, TXN	V_{OL}	-	-	0.4	V
High-Level Output Voltage, (Io=20uA), except TXP, TXN	V_{OH}	(VD+) - 1	-	-	V
Input Leakage Current	I_{in}	-	±1	±10	µA
Differential Input Voltage, RXP to RXN	V_{TH}	200	-	-	mV
Output High Voltage, TXP, TXN (I_{OH} = -30mA)		(VD+) - 0.7	(VD+) - 0.4	-	V
Output Low Voltage, TXP, TXN (I_{OL} = 30mA)		-	0.4	0.7	V

SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+ = 5V, VD+ = 3/5V, ±10%, Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20pF)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width		200	-	-	µs
OMCK Frequency for OMCK = 512*Fso		4.1	-	55.3	MHz
OMCK Low and High Width for OMCK = 512*Fso		7.2	-	-	ns
OMCK Frequency for OMCK = 384*Fso		3.1	-	41.5	MHz
OMCK Low and High Width for OMCK = 384*Fso		10.8	-	-	ns
OMCK Frequency for OMCK = 256*Fso		2.0	-	27.7	MHz
OMCK Low and High Width for OMCK = 256*Fso		14.4	-	-	ns
PLL Clock Recovery Sample Rate Range		8.0	-	108.0	kHz
RMCK output jitter		-	200	-	ps RMS
RMCK output duty cycle		40	50	60	%
RMCK Input Frequency (Note 3)		1.8	-	27.7	MHz
RMCK Input Low and High Width (Note 3)		14.4	-	-	ns
AES3 Transmitter Output Jitter		-	-	1	ns

Notes: 3. PLL is bypassed (Bit RXD0 in Clock Source Control register set to 1), clock is input to the RMCK pin.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS (T_A = 25 °C; VA+ = 5V, VD+ = 3/5V, ±10%, Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20pF)

Parameter		Symbol	Min	Typ	Max	Units
OSCLK Active Edge to SDOUT Output Valid	(Note 4)	t_{dpd}	-	-	20	ns
SDIN Setup Time Before ISCLK Active Edge	(Note 4)	t_{ds}	20	-	-	ns
SDIN Hold Time After ISCLK Active Edge	(Note 4)	t_{dh}	20	-	-	ns
Master Mode						
O/RMCK to I/OSCLK active edge delay	(Note 4)	t_{smd}	0	-	10	ns
O/RMCK to I/OLRCK delay	(Note 5)	t_{lmd}	0	-	10	ns
I/OSCLK and I/OLRCK Duty Cycle			-	50	-	%
Slave Mode						
I/OSCLK Period		t_{sckw}	36	-	-	ns
I/OSCLK Input Low Width		t_{sckl}	14	-	-	ns
I/OSCLK Input High Width		t_{sckh}	14	-	-	ns
I/OSCLK Active Edge to I/OLRCK Edge	(Note 4,5,6)	t_{lrckd}	20	-	-	ns
I/OLRCK Edge Setup Before I/OSCLK Active Edge	(Note 4,5,7)	t_{lrcks}	20	-	-	ns

Notes:
4. The active edges of ISCLK and OSCLK are programmable.
5. The polarity of ILRCK and OLRCK is programmable.
6. This delay is to prevent the previous I/OSCLK edge from being interpreted as the first one after I/OLRCK has changed.
7. This setup time ensures that this I/OSCLK edge is interpreted as the first one after I/OLRCK has changed.

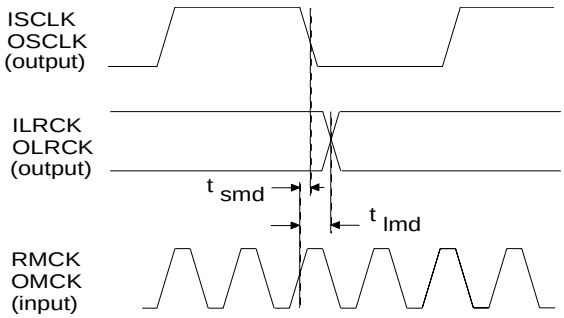


Figure 1. Audio Port Master Mode Timing

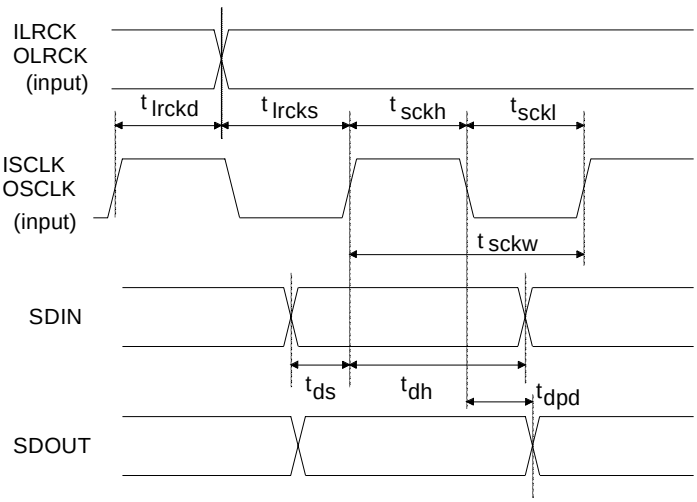


Figure 2. Audio Port Slave Mode and Data Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE (T_A = 25 °C; VA+ = 5V, VD+ = 3/5V, ±10%, Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	(Note 8)	f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 9)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	45	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 10)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 10)	t_{f2}	-	-	100	ns

Notes: 8. If Fso or Fsi is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128Fso and less than 128Fsi. This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 8 kHz, so choosing CCLK to be less than or equal to 1.024 MHz should be safe for all possible conditions.

9. Data must be held for sufficient time to bridge the transition time of CCLK.

10. For f_{sck} <1MHz.

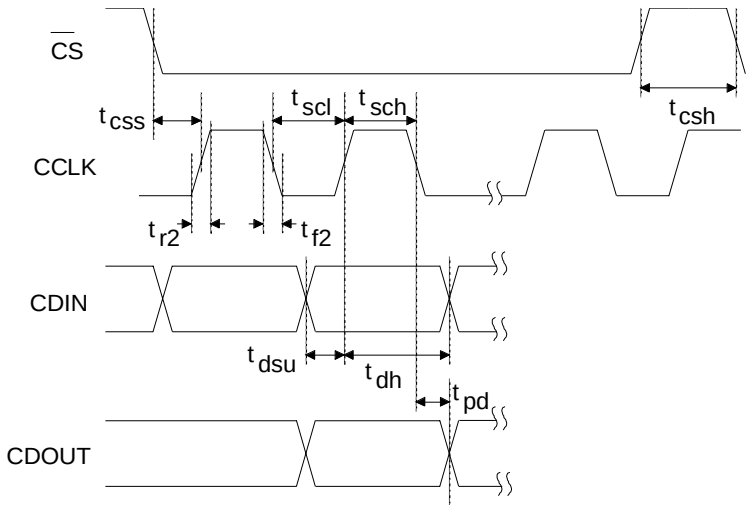


Figure 3. SPI Mode timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C® MODE (Note 11, T_A = 25 °C; VA+ = 5V, VD+ = 3/5V, ±10%, Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20pF)

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency	f_{scl}	-	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	-	µs
Clock Low Time	t_{low}	4.7	-	-	µs
Clock High Time	t_{high}	4.0	-	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	-	µs
SDA Hold Time from SCL Falling (Note 12)	t_{hdd}	0	-	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	-	25	ns
Fall Time of Both SDA and SCL Lines	t_f	-	-	25	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	-	µs

Notes: 11. I²C is a registered trademark of Philips Semiconductors.

12. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

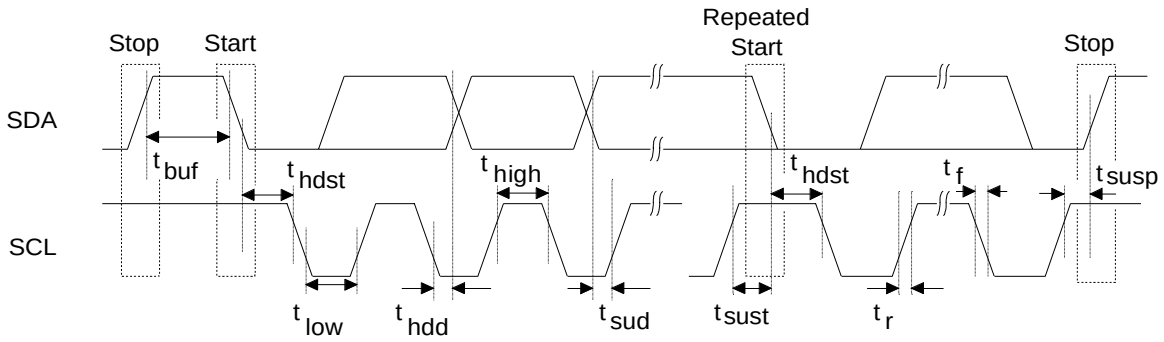
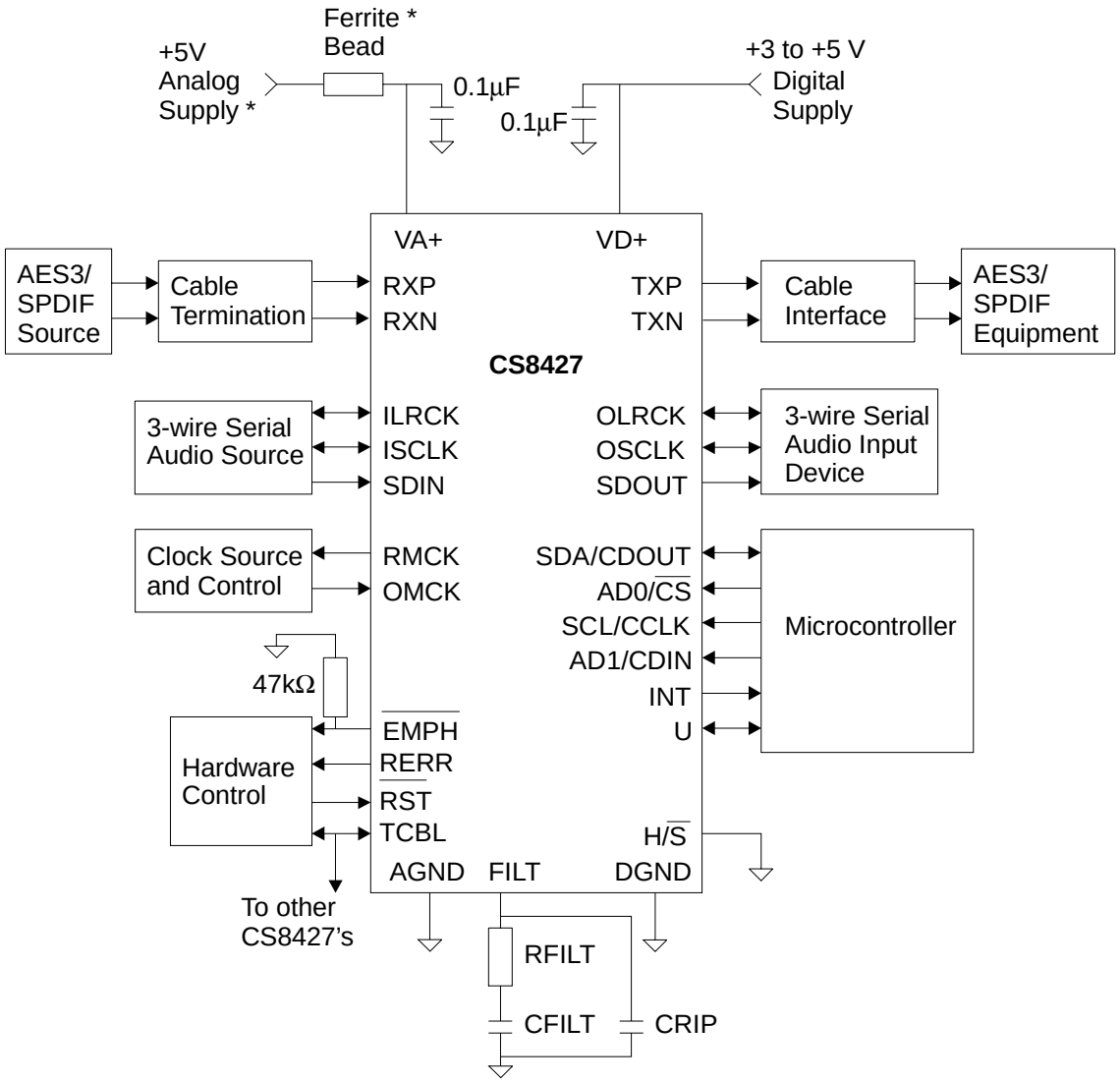


Figure 4. I²C Mode timing

2. TYPICAL CONNECTION DIAGRAM



* A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA+ to VD+ via a ferrite bead. Keep the decoupling capacitor between VA+ and AGND.

Figure 5. Recommended Connection Diagram for Software Mode

3. GENERAL DESCRIPTION

The CS8427 is an AES3 transceiver intended to be used in digital audio systems. Such systems include digital mixing consoles, effects processors, tape recorders and computer multimedia systems.

On the input side of the CS8427, AES3 or a 3-wire serial format can be chosen. The output side produces both AES3 and a 3-wire serial format. An I^2C/SPI compatible microcontroller interface allows full block processing of channel status and user data via block reads from the incoming AES3 data stream and block writes to the outgoing AES3 data stream. The user can also access information decoded from the input AES3 data stream, such as the presence of non-audio data and preemphasis, as well as control the various modes of the device. For users who prefer not to use a micro-controller, a hardware mode has been provided, documented towards the end of this data sheet.

When used for AES3 I/O applications, the CS8427 can automatically transceive user data that conforms to the IEC60958 recommended format. The CS8427 also allows access to the relevant bits in the AES3 data stream to comply with the serial copy management system (SCMS).

The diagram on the cover of this data sheet shows the main functional blocks of the CS8427. Figure 5 shows the supply and external connections to the device.

Familiarity with the AES3 and IEC60958 specifications are assumed throughout this document. The Application Note: "Overview of Digital Audio Interface Data Structures" contains a tutorial on digital audio specifications. The paper "An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission", by Clif Sanchez, is an excellent tutorial on SCMS. It may be obtained from Cirrus Logic, or from the AES.

To guarantee system compliance, the proper standards documents should be obtained. The latest AES3 standard should be obtained from the Audio Engineering Society or ANSI, the latest IEC60958 standard from the International Electrotechnical Commission and the latest EIAJ CP-1201 standard from the Japanese Electronics Bureau.

4. DATA I/O FLOW AND CLOCKING OPTIONS

The CS8427 can be configured for several connectivity alternatives, called data flows. Figure 10 shows the data flow switching, along with the control register bits which control the switches; this drawing only shows the audio data paths for simplicity. Users should note that not all the possible data flow switch setting combinations are valid, because of the clock distribution architecture.

The AESBP switch allows a TTL level, already biphase mark encoded, data stream connected to RXP to be routed to the TXP and TXN pin drivers. The TXOFF switch causes the TXP and TXN outputs to be driven to ground.

There are two possible clock sources. The first is known as the recovered clock, is the output of a PLL, and is connected to the RMCK pin. The input to the PLL can be either the incoming AES3 data stream or the ILRCK word rate clock from the serial audio input port. The second clock is input via the OMCK pin and would normally be a crystal derived stable clock. The Clock Source Control Register bits determine which clock is used to operate the CS8427.

By studying the following drawings and appropriately setting the Data Flow Control and Clock Source Control register bits, the CS8427 can be configured to fit a variety of customer requirements. Please note that applications implementing both the Serial Audio Output Port and the AES3 Transmitter must operate at the same sample rate because they are both controlled by the same clock source.

Figure 12 shows the entire data path clocked via the PLL generated recovered clock. Figure 13 illustrates a standard AES3 receiver function. Figure 14 shows a standard AES3 transmitter function.

4.1 AES3 Transmitter and Receiver

The CS8427 includes an AES3 digital audio receiver and an AES3 digital audio transmitter. A comprehensive buffering scheme provides read/write access to the channel status and user data. This buffering scheme is described in the Appendix: Channel Status and User Data Buffer Management.

4.2 AES3 Receiver

The AES3 receiver accepts and decodes audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. The receiver consists of a differential input stage, accessed via pins RXP and RXN, a PLL based clock recovery circuit, and a decoder which separates the audio data from the channel status and user data.

External components are used to terminate and isolate the incoming data cables from the CS8427. These components are detailed in the Appendix "External AES/SPDIF/IEC60958 Transmitter and Receiver Components".

4.2.1 PLL, Jitter Attenuation, Varispeed

An on-chip Phase Locked Loop (PLL) is used to recover the clock from the incoming data stream. In some applications, low jitter in the recovered clock, presented on the RMCK pin, is important. For this reason, the PLL has been designed to have good jitter attenuation characteristics, shown in Figures 6 & 7. In addition, the PLL has been designed to only use the preambles of the AES3 stream to provide lock update information to the PLL. This results in the PLL being immune to data dependent jitter effects, since the AES3 preambles do not vary with the data. The PLL has the ability to lock onto a wide range of input sample rates with no external component changes. If the sample rate of the input subsequently changes, for example in a varispeed application, the PLL will only track up to ±12.5% from the nominal center sample rate. The nominal center sample rate is the sample rate that the PLL first locks onto upon application of an AES3 data stream or after enabling the CS8427 clocks by setting the RUN control bit. If the 12.5% sample rate limit is exceeded, the PLL will return to its wide lock range mode and re-acquire a new nominal center sample rate.

4.2.2 OMCK System Clock Mode

A special clock switching mode is available that allows the clock that is input through the OMCK pin to be output through the RMCK pin. This feature is controlled by the SWCLK bit in register 1 of the control registers. When the PLL loses lock, the frequency of the VCO drops to 300 kHz. The clock switching mode allows the clock input through OMCK to be used as a clock in the system without any disruption when the PLL loses lock, for example, when the input is removed from the receiver. When SWCLK is enabled and this mode is implemented, RMCK is an output and is not bi-directional. Please note that internal circuitry associated with RMCK is not driven by OMCK.

4.2.3 PLL External Components

The PLL behavior is affected by the external filter component values. Figure 5 shows the recommended configuration of the two capacitors and one resistor required. There are two sets of component values recommended, depending on whether the AES3 receiver or ILRCK is used and the respective sample rate used in the application, see Tables 1 & 2. Lock times are calculated as worst case for an Fsi transition of 96kHz. The application note, AN159: "PLL Filter Optimization for the CS8415A, CS8420, and CS8427" provides further resources for the PLL.

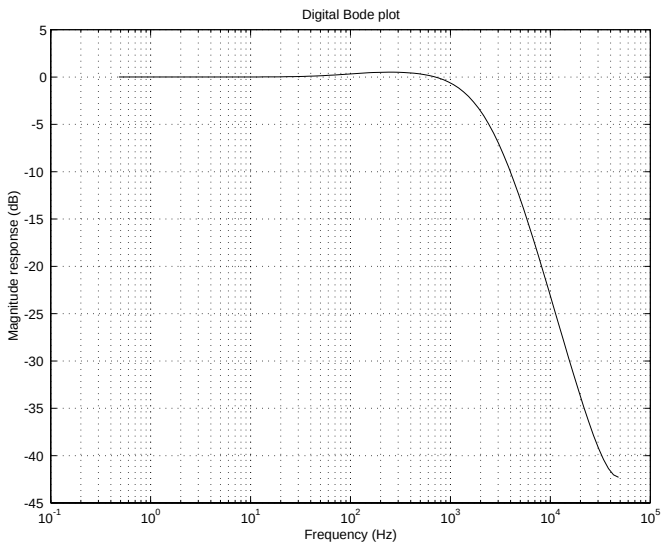


Figure 6. Jitter Attenuation Characteristics of PLL with 8 to 96 kHz Fs Filter Components-AES3

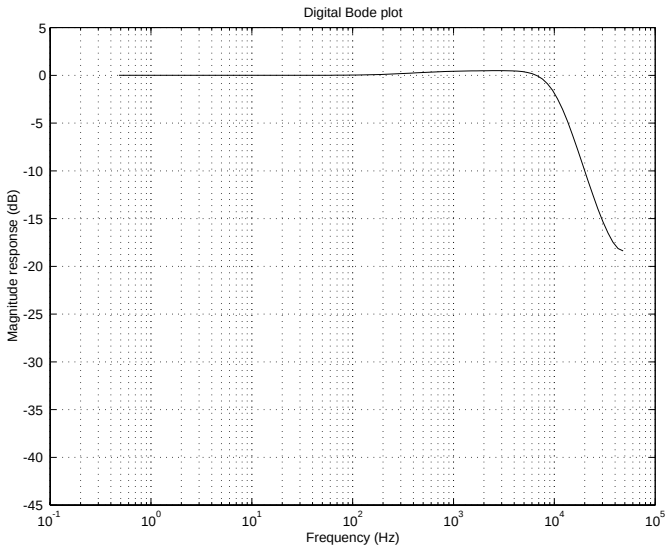


Figure 7. Jitter Attenuation Characteristics of PLL with 32 to 96 kHz Fs Filter Components-AES3

Fsi Range (kHz)	RFILT (kΩ)	CFILT (µF)	CRIP (nF)	PLL Lock Time (ms)
8 to 96	0.909	2.2	33	56
32 to 96	5	0.082	2.2	15

Table 1. PLL External Components using AES3 Receiver

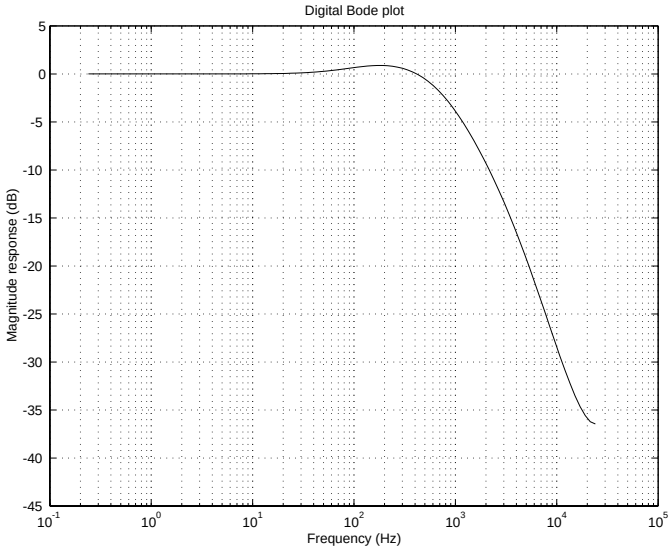


Figure 8. Jitter Attenuation Characteristics of PLL with 8 to 96 kHz Fs Filter Components-ILRCK

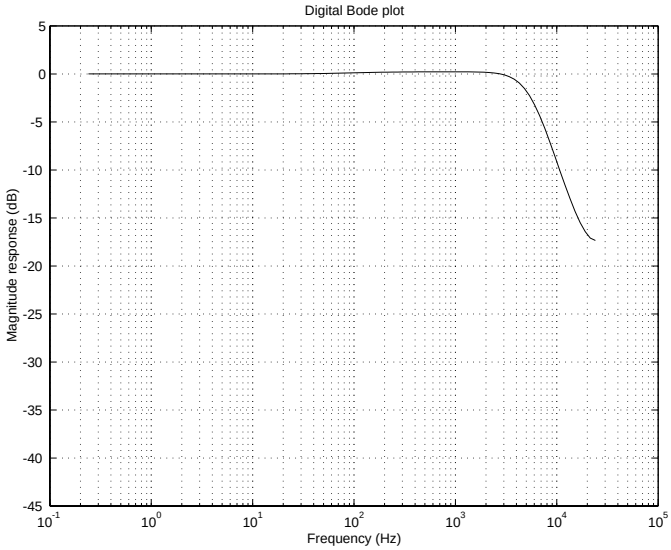


Figure 9. Jitter Attenuation Characteristics of PLL with 32 to 96 kHz Fs Filter Components-ILRCK

Fsi Range (kHz)	RFILT (kΩ)	CFILT (µF)	CRIP (nF)	PLL Lock Time (ms)
8 to 96	0.909	2.2	33	56
32 to 96	5.1	150	3.9	15

Table 2. PLL External Components using ILRCK

4.2.4 Error Reporting and Hold Function

While decoding the incoming AES3 data stream, the CS8427 can identify several kinds of error, indicated in the Receiver Error register. The UNLOCK bit indicates whether the PLL is locked to the incoming AES3 data. The V bit reflects the current validity bit status. The CONF (confidence) bit indicates the amplitude of the eye pattern opening, indicating a link that is close to generating errors. The BIP (bi-phase) error bit indicates an error in incoming bi-phase coding. The PAR (parity) bit indicates a received parity error.

The error bits are "sticky": they are set on the first occurrence of the associated error and will remain set until the user reads the register via the control port. This enables the register to log all unmasked errors that occurred since the last time the register was read.

The Receiver Error Mask register allows masking of individual errors. The bits in this register serve as masks for the corresponding bits of the Receiver Error Register. If a mask bit is set to 1, the error is considered unmasked, which implies the following: its occurrence will be reported in the receiver error register, induce a pulse on RERR, invoke the occurrence of a RERR interrupt, and affect the current audio sample according to the status of the HOLD bits. The HOLD bits allow a choice of holding the previous sample, replacing the current sample with zero (mute), or not changing the current audio sample. If a mask bit is set to 0, the error is considered masked, which implies the following: its occurrence will not be reported in the receiver error register, will not induce a pulse on RERR or generate a RERR interrupt, and will not affect the current audio sample. The QCRC and CCRC errors do not affect the current audio sample, even if unmasked.

4.2.5 Channel Status Data Handling

The first two bytes of the Channel Status block are decoded into the Receiver Channel Status register. The setting of the CHS bit in the Channel Status Data Buffer Control register determines whether the channel status decodes are from the A channel (CHS = 0) or B channel (CHS = 1).

The PRO (professional) bit is extracted directly. For consumer data, the COPY (copyright) bit is extracted, and the category code and L bits are decoded to determine SCMS status, indicated by the ORIG (original) bit. Finally, the $\overline{\text{AUDIO}}$ bit is extracted and used to set an $\overline{\text{AUDIO}}$ indicator, as described in the Non-Audio Auto-Detection section below.

If 50/15 µs pre-emphasis is detected, the state of the $\overline{\text{EMPH}}$ pin is adjusted accordingly.

The encoded channel status bits which indicate sample word length are decoded according to AES3-1992 or IEC 60958. Audio data routed to the serial audio output port is unaffected by the word length settings; all 24 bits are passed on as received.

The Appendix: Channel Status and User Data Buffer Management (page 51) describes the overall handling of Channel Status and User data.

4.2.6 User Data Handling

The incoming user data is buffered in a user accessible buffer. Various automatic modes of re-transmitting received User data are provided. The Appendix: Channel Status and User Data Buffer Management describes the overall handling of CS and U data.

Received User data may also be output to the U pin, under the control of a control register bit. Depending on the data flow and clocking options selected, there may not be a clock available to qualify the U data output. Figure 15 illustrates the timing.

If the incoming user data bits have been encoded as Q-channel subcode, the data is decoded and presented in ten consecutive register locations. An interrupt may be enabled to indicate the decoding of a new Q-channel block, which may be read via the control port.

4.2.7 Non-Audio Auto-Detection

An AES3 data stream may be used to convey non-audio data, thus it is important to know whether the incoming AES3 data stream is digital audio or not. This information is typically conveyed in channel status bit 1 ($\overline{\text{AUDIO}}$), which is extracted automatically by the CS8427. However, certain non-audio sources, such as AC3 or MPEG encoders, may not adhere to this convention, and the bit may not be properly set. The CS8427 AES3 receiver can detect such non-audio data. This is accomplished by looking for a 96-bit sync code, consisting of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872, and 0x4E1F. When the sync code is detected, an internal AUTODETECT signal will be asserted. If no additional sync codes are detected within the next 4096 frames, AUTODETECT will be de-asserted until another sync code is detected. The $\overline{\text{AUDIO}}$ bit in the Receiver Channel Status register is the logical OR of AUTODETECT and the received channel status bit 1. If non-audio data is detected, the data is still processed exactly as if it were normal audio. It is up to the user to mute the outputs as required.

4.3 AES3 Transmitter

The AES3 transmitter encodes and transmits audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. Audio and control data are multiplexed together and bi-phase mark encoded. The resulting bit stream is driven to an output connector either directly or through a transformer.

The transmitter clock may be derived from the clock input pin OMCK, or from the incoming data. If OMCK is asynchronous to the data source, an interrupt bit is provided that will go high every time a data sample is dropped or repeated.

The channel status (C) and user channel (U) bits in the transmitted data stream are taken from storage areas within the CS8427. The user can manually access the internal storage or configure the CS8427 to run in one of several automatic modes. The Appendix: Channel Status and User Data Buffer Management provides detailed descriptions of each automatic mode and describes methods of manually accessing the storage areas. The transmitted user data can optionally be input via the U pin, under the control of a control port register bit. Figure 15 shows the timing requirements for inputting U data via the U pin.

4.3.1 Transmitted Frame and Channel Status Boundary Timing

The TCBL pin is used to control or indicate the start of transmitted channel status block boundaries and may be used as an input or output.

In some applications, it may be necessary to control the precise timing of the transmitted AES3 frame boundaries. This may be achieved in three ways:

a) With TCBL set to input, driving TCBL high for >3 OMCK clocks will cause a frame start, as well as a new channel status block start.

b) If the AES3 output comes from the AES3 input, setting TCBL as output will cause AES3 output frame boundaries to align with AES3 input frame boundaries.

c) If the AES3 output comes from the serial audio input port while the port is in slave mode and TCBL is set to output, the start of the A channel sub-frame will be aligned with the leading edge of ILRCK.

4.3.2 TXN and TXP Drivers

The line drivers are low skew, low impedance, differential outputs capable of driving cables directly. Both drivers are set to ground during reset ($\overline{RST}$ = low), when no AES3 transmit clock is provided, and optionally under the control of a register bit. The CS8427 also allows immediate mute of the AES3 transmitter audio data via a control register bit.

External components are used to terminate and isolate the external cable from the CS8427. These components are detailed in the Appendix "External AES/SPDIF/IEC60958 Transmitter and Receiver Components".

4.4 Mono Mode Operation

The AES3 standard is currently being updated to include options for 96kHz sample rate operation. One method is to double the frame rate of the current format. This results in a stereo signal with a sample rate of 96 kHz, carried over a single twisted pair cable. An alternate method is implemented using the two sub-frames in a 48kHz frame rate AES3 signal to carry consecutive samples of a mono signal, resulting in a 96kHz sample rate stream. This allows older equipment, whose AES3 transmitters and receivers are not rated for 96kHz frame rate operation, to handle 96kHz sample rate information. In this "mono mode", two AES3 cables are needed for stereo data transfer. The CS8427 offers mono mode operation for the AES3 receiver and the AES3 transmitter. The receiver and transmitter sections may be independently set to mono mode via the MMR and MMT control bits.

4.4.1 Receiver Mono Mode

The receiver mono mode effectively doubles the input frame rate, Fsi. The clock output on the RMCK pin tracks Fsi, and thus is doubled in frequency compared to stereo mode. The receiver will run at a frame rate of Fsi/2, and the serial audio output port will run at Fsi. Sub-frame A data will be routed to both the left and right data fields on SDOUT. Similarly, sub-frame B data will be routed to both the left and right data fields of the next word clock cycle of SDOUT.

Using receiver mono mode is only necessary if the serial audio output port must run at 96kHz. If the CS8427 is kept in normal stereo mode and receives AES3 data arranged in mono mode, the serial audio output port will run at 48kHz, with left and right data fields representing consecutive audio samples.

4.4.2 Transmitter Mono Mode

In transmitter mono mode, the input port will run at the audio sample rate (Fso), while the AES3 transmitter frame rate will be at Fso/2. Consecutive left or right channel serial audio data samples may be selected for transmission via the A and B subframes, and the channel status block transmitted is also selectable.

Using transmitter mono mode is only necessary if the incoming audio sample rate is already at 96kHz and contains both left and right audio data words. The "mono mode" AES3 output stream may also be achieved by keeping the CS8427 in normal stereo mode and placing consecutive audio samples in the left and right positions of an incoming data stream with a 48kHz word rate.

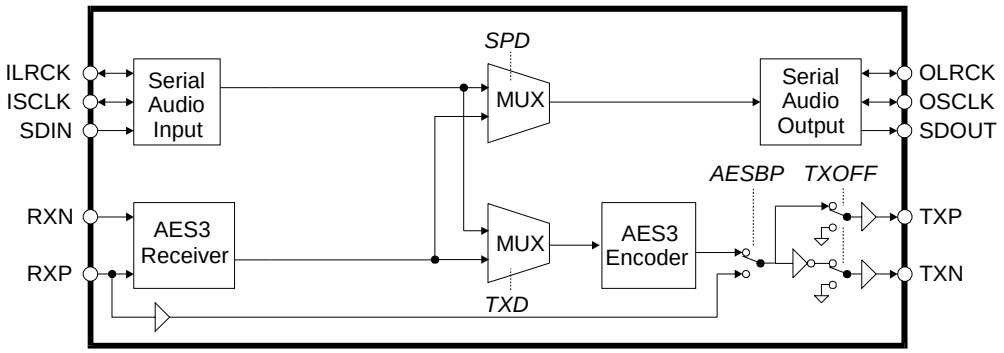
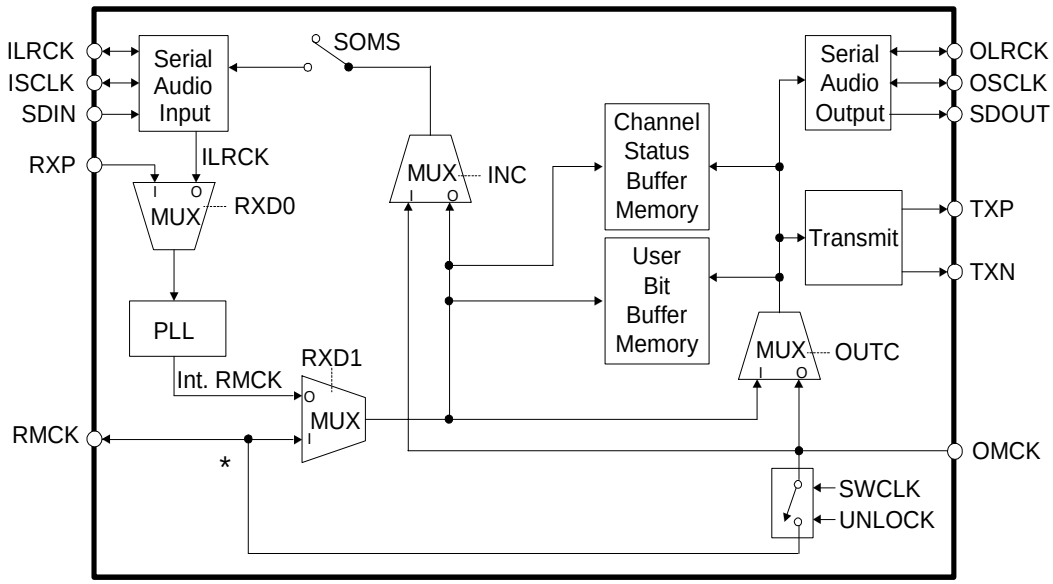
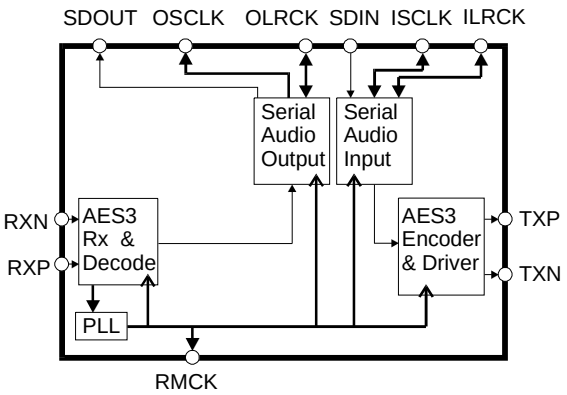


Figure 10. Software Mode Audio Data Flow Switching Options



* Note: When SWCLK mode is enabled, signal input on OMCK is only output through RMCK and not routed back through the RXD1 multiplexer; RMCK is not bi-directional in this mode.

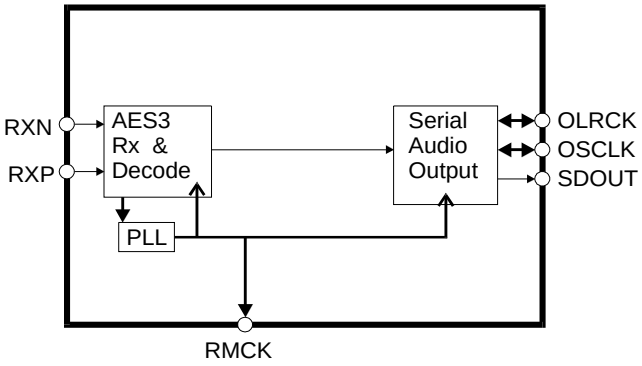
Figure 11. CS8427 Clock Routing



Data Flow Control Bits		Clock Source Control Bits	
TXD1-0:	01	*OUTC:*	1
SPD1-0:	10	*INC:*	0
SRCD:	1	*RXD1-0:*	01

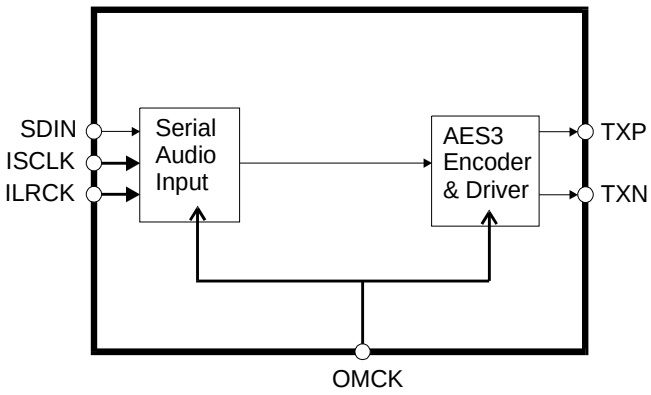
NOTE: applications implementing both the Serial Audio Output Port and the AES3 Transmitter must operate at the same sample rate because they are both controlled by the same clock source.

Figure 12. AES3 Input to Serial Audio Output, Serial Audio Input to AES3 Out



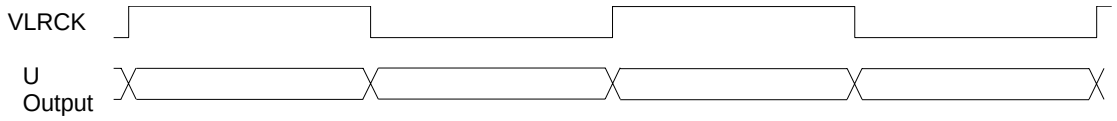
Data Flow Control Bits		Clock Source Control Bits	
TXD1-0:	10	*OUTC:*	1
SPD1-0:	10	*INC:*	0
SRCD:	0	*RXD1-0:*	01

Figure 13. AES3 Input to Serial Audio Output Only



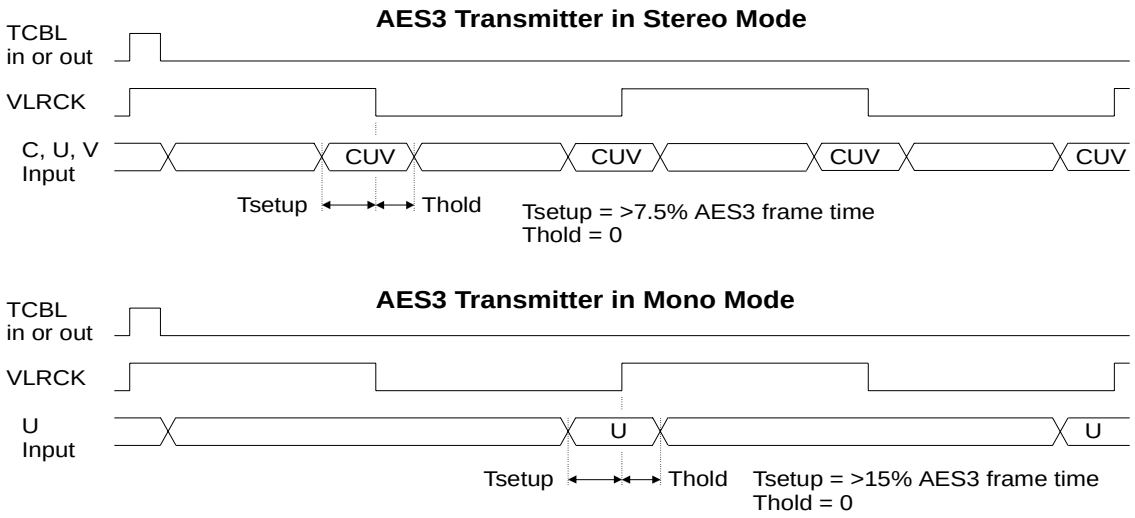
Data Flow Control Bits		Clock Source Control Bits	
TXD1-0:	01	*OUTC:*	0
SPD1-0:	01	*INC:*	1
SRCD:	0	*RXD1-0:*	00

Figure 14. Input Serial Port to AES3 Transmitter



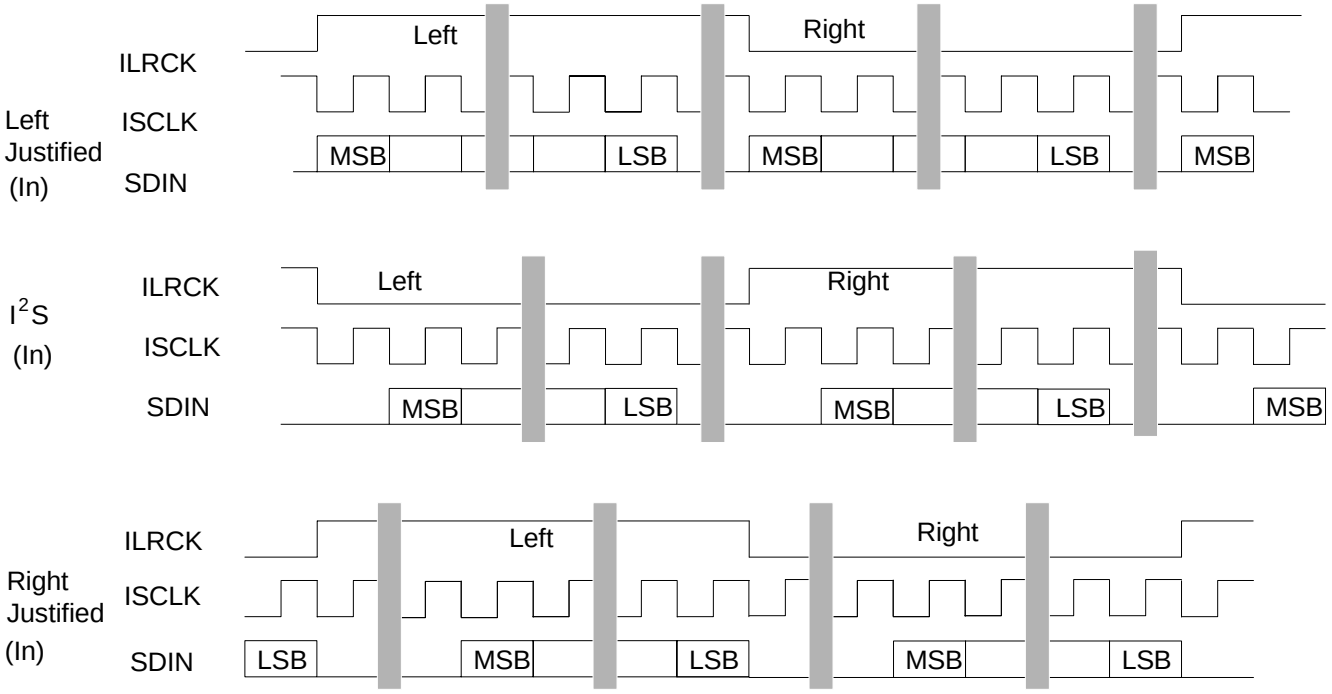
VLRCK is a virtual word clock, which may not exist, but is used to illustrate the U timing.
VLRCK duty cycle is 50%. VLRCK frequency is always equal to the incoming frame rate.
If the serial audio output port is in master mode, VLRCK = OLRCK.
If the serial audio output port is in slave mode, then VLRCK needs to be externally created, if required.
U transitions are aligned within ±1% of VLRCK period to VLRCK edges

Figure 15. AES3 Receiver Timing for U pin output data



VLRCK is a virtual word clock, which may not exist, but is used to illustrate the CUV timing.
VLRCK duty cycle is 50%.
In stereo mode, VLRCK = AES3 frame rate. In mono mode, VLRCK = 2*AES3 frame rate
If the serial audio output port is in master mode, and TCBL is an output,
then VLRCK = OLRCK.
If the serial audio input port is in master mode, and TCBL is an input, then VLRCK = ILRCK.
Otherwise, VLRCK needs to be externally created, if required

Figure 16. AES3 Transmitter Timing for C, U and V pin input data



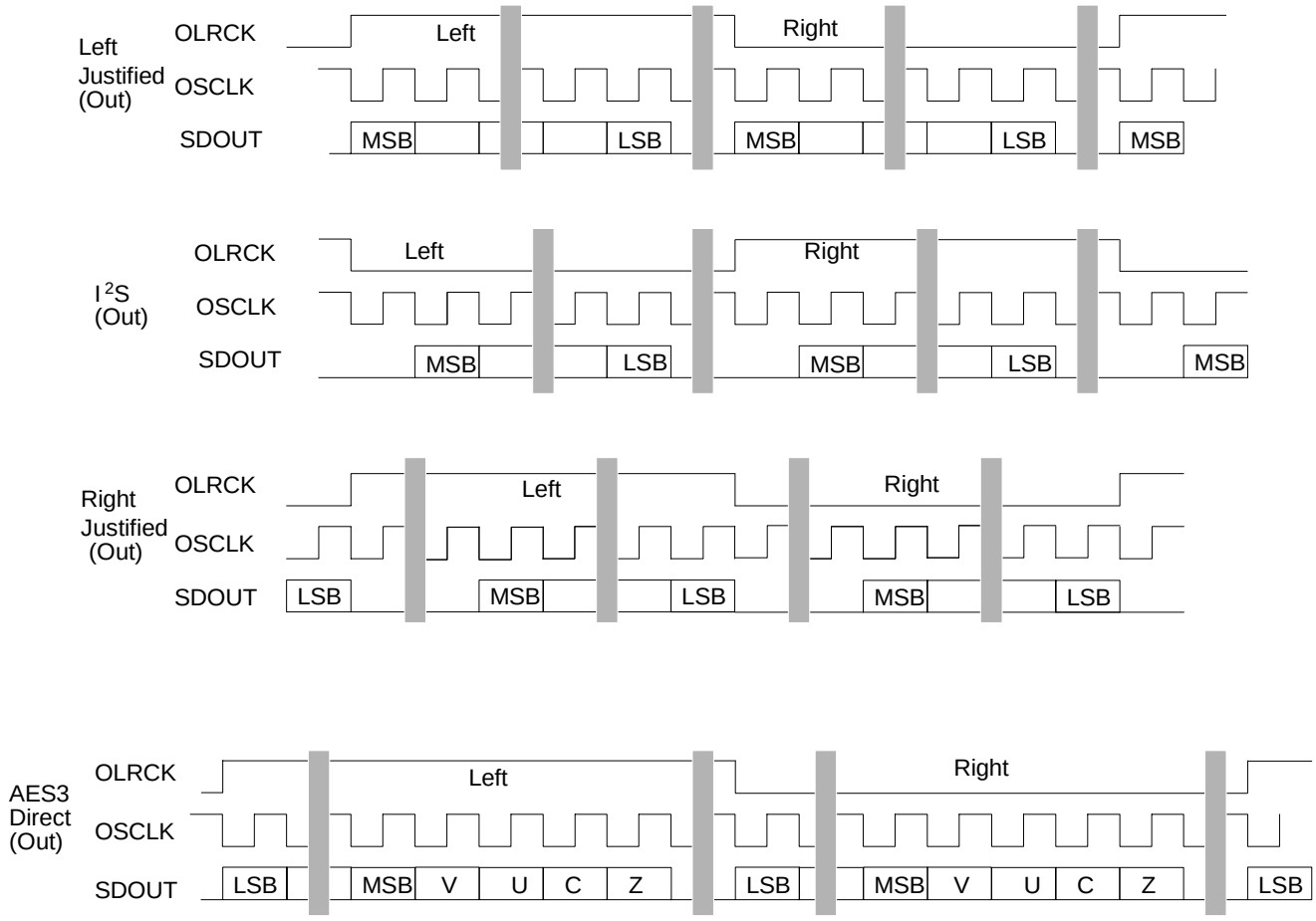
	SIMS*	SISF*	SIRES1/0*	SIJUST*	SIDEL*	SISPOL*	SILRPOL*
Left Justified	X	X	00	0	0	0	0
I^2S	X	X	00+	0	1	0	1
Right Justified	X	X	XX	1	0	0	0

X = don't care to match format, but does need to be set to the desired setting

+ I^2S can accept an arbitrary number of bits, determined by the number of ISCLK cycles

* See Serial Input Port Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 17. Serial Audio Input Example Formats



	SOMS*	SOSF*	SORES1/0*	SOJUST*	SODEL*	SOSPOL*	SOLRPOL*
Left Justified	X	X	XX	0	0	0	0
I^2S	X	X	XX	0	1	0	1
Right Justified	1	X	XX	1	0	0	0
AES3 Direct	X	X	11	0	0	0	0

X = don't care to match format, but does need to be set to the desired setting

* See Serial Output Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 18. Serial Audio Output Example Formats

5. CONTROL PORT DESCRIPTION AND TIMING

The control port is used to access the registers, allowing the CS8427 to be configured for the desired operational modes and formats. In addition, Channel Status and User data may be read and written via the control port. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I^2C, with the CS8427 acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/$\overline{CS}$ pin after the $\overline{RST}$ pin has been brought high. I^2C mode is selected by connecting the AD0/$\overline{CS}$ pin to VD+ or DGND, thereby permanently selecting the desired AD0 bit address state.

5.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS8427 chip select signal; CCLK is the control port bit clock (input into the CS8427 from the microcontroller); CDIN is the input data line from the microcontroller; CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 19 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, then the MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address, and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

5.2 I^2C Mode

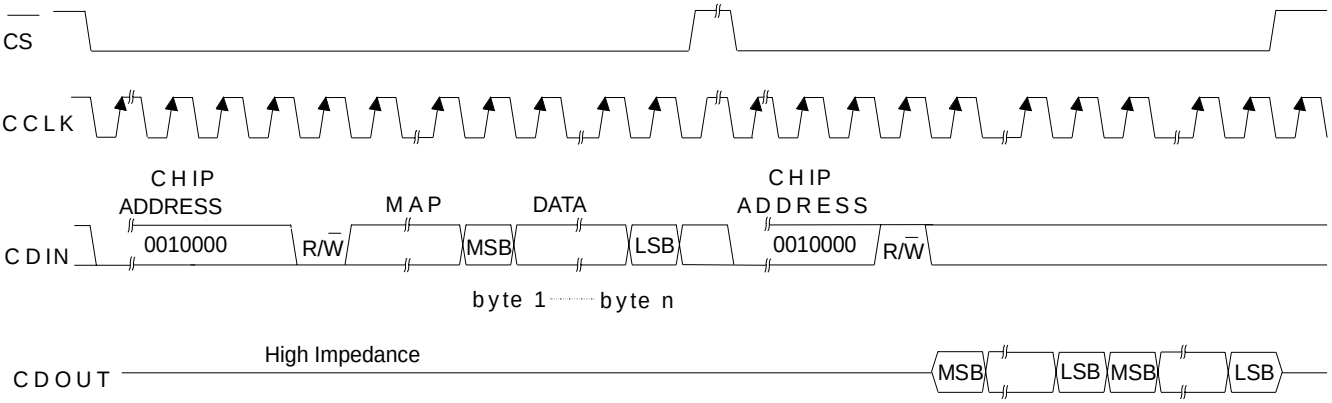
In I^2C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by SCL, with the clock to data relationship as shown in Figure 20. There is no $\overline{CS}$ pin. Each individual CS8427 is given a unique address. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected to VD+ or DGND as desired. The $\overline{EMPH}$ pin is used to set the AD2 bit, by connecting a resistor from the $\overline{EMPH}$ pin to VD+ or to DGND. The state of the pin is sensed while the CS8427 is being reset. The upper four bits of the seven bit address field are fixed at 0010. To communicate with a CS8427, the chip address field, which is the first byte sent to the CS8427, should be 0010 followed by the settings of the $\overline{EMPH}$, AD1, and AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an ac-

knowledge bit, ACK, which is output from the CS8427 after each input byte is read. The ACK bit is input to the CS8427 from the microcontroller after each transmitted byte. I^2C is a registered trademark of Philips Semiconductors.

5.3 Interrupts

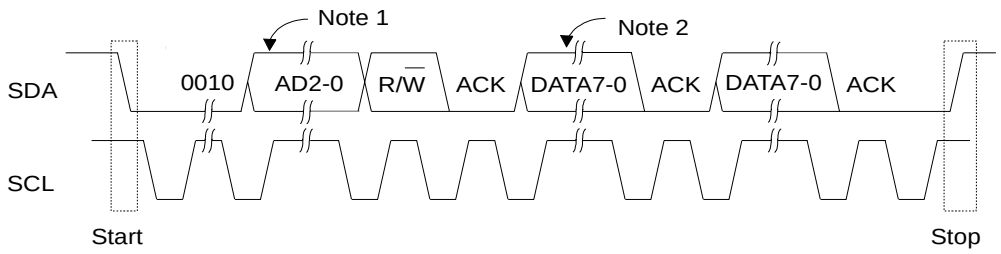
The CS8427 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active low, active high, or active low with no active pull-up transistor. This last mode is used for active low, wired-OR hookups with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. Each source may be masked off via mask registers. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different set-ups are possible depending on the needs of the equipment designer.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 19. Control Port Timing in SPI Mode



Note 1: AD2 is derived from a resistor attached to the EMPH pin, AD1 and AD0 are determined by the state of the corresponding pins

Note 2: If operation is a write, this byte contains the Memory Address Pointer, MAP

Figure 20. Control Port Timing in I^2C Mode

6. CONTROL PORT REGISTER SUMMARY

Addr	Function	7	6	5	4	3	2	1	0
0	Reserved	0	0	0	0	0	0	0	0
1	Control 1	SWCLK	VSET	MUTESAO	MUTEAES	0	INT1	INT0	TCBLD
2	Control 2	0	HOLD1	HOLD0	RMCKF	MMR	MMT	MMTCS	MMTLR
3	Data Flow Control	0	TXOFF	AESBP	TXD1	TXD0	SPD1	SPD0	0
4	Clock Source Control	0	RUN	CLK1	CLK0	OUTC	INC	RXD1	RXD0
5	Serial Input Format	SIMS	SISF	SIRES1	SIRES0	SIJUST	SIDEL	SISPOL	SILRPOL
6	Serial Output Format	SOMS	SOSF	SORES1	SORES0	SOJUST	SODEL	SOSPOL	SOLRPOL
7	Interrupt 1 Status	TSLIP	OSLIP	0	0	0	DETC	EFTC	RERR
8	Interrupt 2 Status	0	0	0	0	DETU	EFTU	QCH	0
9	Interrupt 1 Mask	TSLIPM	OSLIPM	0	0	0	DETCM	EFTCM	RERRM
10	Interrupt 1 Mode (MSB)	TSLIP1	OSLIP1	0	0	0	DETC1	EFTC1	RERR1
11	Interrupt 1 Mode (LSB)	TSLIP0	OSLIP0	0	0	0	DETC0	EFTC0	RERR0
12	Interrupt 2 Mask	0	0	0	0	DETUM	EFTUM	QCHM	0
13	Interrupt 2 Mode (MSB)	0	0	0	0	DETU1	EFTU1	QCH1	0
14	Interrupt 2 Mode (LSB)	0	0	0	0	DETU0	EFTU0	QCH0	0
15	Receiver CS Data	AUX3	AUX2	AUX1	AUX0	PRO	$\overline{\text{AUDIO}}$	COPY	ORIG
16	Receiver Errors	0	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR
17	Receiver Error Mask	0	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM
18	CS Data Buffer Control	0	0	BSEL	CBMR	DETCI	EFTCI	CAM	CHS
19	U Data Buffer Control	0	0	0	UD	UBM1	UBM0	DETUI	EFTUI
20-29	Q sub-code Data								
30	OMCK/RMCK Ratio	ORR7	ORR6	ORR5	ORR4	ORR3	ORR2	ORR1	ORR0
31	Reserved	0	0	0	0	0	0	0	0
32-55	C or U Data Buffer								
127	ID and Version	ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

Table 3. Control Register Map Summary

6.1 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

INCR *- Auto Increment Address Control Bit*

Default = '0'

0 - Disable

1 - Enable

MAP6:MAP0 *- Register address*

Note: Reserved registers must not be written to during normal operation. Some reserved registers are used for test modes, which can completely alter the normal operation of the CS8427.

7. CONTROL PORT REGISTER BIT DEFINITIONS

7.1 Control 1 (1)

7	6	5	4	3	2	1	0
SWCLK	VSET	MUTESAO	MUTEAES	0	INT1	INT0	TCBLD

SWCLK *- Controls output of OMCK on RMCK when PLL loses lock*

Default = '0'

0 - RMCK default function

1 - OMCK output on RMCK pin

VSET *- Transmitted V bit level*

Default = '0'

0 - Indicates data is valid, linear PCM audio data

1 - Indicates data is invalid or not linear PCM audio data

MUTESAO *- Mute control for the serial audio output port*

Default = '0'

0 - Disabled

1 - Enabled

MUTEAES *- Mute control for the AES transmitter output*

Default = '0'

0 - Disabled

1 - Enabled

INT1:INT0 *- Interrupt output pin (INT) control*

Default = '00'

00 - Active high; high output indicates interrupt condition has occurred

01 - Active low, low output indicates an interrupt condition has occurred

10 - Open drain, active low. Requires an external pull up resistor on the INT pin.

11 - Reserved

TCBLD *- Transmit Channel Status Block pin (TCBL) direction specifier*

Default = '0'

0 - TCBL is an input

1 - TCBL is an output

7.2 Control 2 (2)

7	6	5	4	3	2	1	0
0	HOLD1	HOLD0	RMCKF	MMR	MMT	MMTCS	MMTLR

HOLD1:HOLD0 *- Determine how received audio sample is affected when a receiver error occurs*

Default = '00'

00 - Hold the last valid audio sample

01 - Replace the current audio sample with 00 (mute)

10 - Do not change the received audio sample

11 - Reserved

RMCKF *- Select recovered master clock output pin frequency.*

Default = '0'

0 - RMCK is equal to 256 * Fsi

1 - RMCK is equal to 128 * Fsi

MMR *- Select AES3 receiver mono or stereo operation*

Default = '0'

0 - Normal stereo operation

1 - A and B subframes treated as consecutive samples of one channel of data. Data is duplicated to both left and right parallel outputs of the AES receiver block. The input sample rate (Fsi) is doubled compared to MMR=0

MMT *- Select AES3 transmitter mono or stereo operation*

Default = '0'

0 - Normal stereo operation

1 - Output either left or right channel inputs into consecutive subframe outputs (mono mode, left or right is determined by MMTLR bit)

MMTCS *- Select A or B channel status data to transmit in mono mode*

Default = '0'

0 - Use channel A CS data for the A subframe and use channel B CS data for the B subframe

1 - Use the same CS data for both the A and B subframe outputs. If MMTLR = 0, use the left channel CS data. If MMTLR = 1, use the right channel CS data.

MMTLR *- Channel Selection for AES Transmitter mono mode*

Default = '0'

0 - Use left channel input data for consecutive subframe outputs

1- Use right channel input data for consecutive subframe outputs

7.3 Data Flow Control (3)

7	6	5	4	3	2	1	0
0	TXOFF	AESBP	TXD1	TXD0	SPD1	SPD0	0

The Data Flow Control register configures the flow of audio data to/from the following blocks: Serial Audio Input Port, Serial Audio Output Port, AES3 receiver, and AES3 transmitter. In conjunction with the Clock Source Control register, multiple Receiver/Transmitter/Transceiver modes may be selected. The output data should be muted prior to changing bits in this register to avoid transients.

TXOFF *- AES3 Transmitter Output Driver Control*

Default = ‘0

0 - AES3 transmitter output pin drivers normal operation

1 - AES3 transmitter output pin drivers drive to 0V.

AESBP *- AES3 bypass mode selection*

Default = ‘0’

0 - Normal operation

1 - Connect the AES3 transmitter driver input directly to the RXP pin, which becomes a normal TTL threshold digital input.

TXD1:TXD0 *- AES3 Transmitter Data Source*

Default = ‘01’

00 - Reserved

01 - Serial audio input port

10 - AES3 receiver

11 - Reserved

SPD1:SPD0 *- Serial Audio Output Port Data Source*

Default = ‘10’

00 - Reserved

01 - Serial Audio Input Port

10 - AES3 receiver

11 - Reserved

7.4 Clock Source Control (4)

7	6	5	4	3	2	1	0
0	RUN	CLK1	CLK0	OUTC	INC	RXD1	RXD0

This register configures the clock sources of various blocks. In conjunction with the Data Flow Control register, various Receiver/Transmitter/Transceiver modes may be selected.

RUN - *Controls the internal clocks, allowing the CS8427 to be placed in a "powered down", low current consumption, state.*

Default = '0'

0 - Internal clocks are stopped. Internal state machines are reset. The fully static control port is operational, allowing registers to be read or changed. Reading and writing the U and C data buffers is not possible. Power consumption is low.

1 - Normal part operation. This bit must be written to the 1 state to allow the CS8427 to begin operation. All input clocks should be stable in frequency and phase when RUN is set to 1.

CLK1:0 - *Output side master clock input (OMCK) frequency to output sample rate (Fso) ratio selector. If these bits are changed during normal operation, then always stop the CS8427 first (RUN = 0), write the new value, then start the CS8427 (RUN = 1).*

Default = '00'

00 - OMCK frequency is 256*Fso

01 - OMCK frequency is 384*Fso

10 - OMCK frequency is 512*Fso

11 - Reserved

OUTC - *Output Time Base*

Default = '0'

0 - OMCK input pin, modified by the selected divide ratio bits CLK1:0.

1 - Recovered Input Clock

INC - *Input Time Base Clock Source*

Default = '0'

0 - Recovered Input Clock

1 - OMCK input pin, modified by the selected divide ratio bits CLK1:0.

RXD1:0 - *Recovered Input Clock Source*

Default = '00'

00 - 256*Fsi, where Fsi is derived from the ILRCK pin (only possible when the serial audio input port is in slave mode)

01 - 256*Fsi, where Fsi is derived from the AES3 input frame rate

10 - Bypass the PLL and apply an external 256*Fsi clock via the RMCK pin. The AES3 receiver is held in synchronous reset. This setting is useful to prevent UNLOCK interrupts when using an external RMCK and inputting data via the serial audio input port.

11 - Bypass the PLL and apply an external 256*Fsi clock via the RMCK pin. The AES3 receiver is operational.

7.5 Serial Audio Input Port Data Format (5)

7	6	5	4	3	2	1	0
SIMS	SISF	SIRES1	SIRES0	SIJUST	SIDEL	SISPOL	SILRPOL

SIMS *- Master/Slave Mode Selector*

Default = '0'
0 - Serial audio input port is in slave mode
1 - Serial audio input port is in master mode

SISF *- ISCLK frequency (for master mode)*

Default = '0'
0 - 64*Fsi
1 - 128*Fsi

SIRES1:0 *- Resolution of the input data, for right-justified formats*

Default = '00'
00 - 24 bit resolution
01 - 20 bit resolution
10 - 16 bit resolution
11 - Reserved

SIJUST *- Justification of SDIN data relative to ILRCK*

Default = '0'
0 - Left-justified
1 - Right-justified

SIDEL *- Delay of SDIN data relative to ILRCK, for left-justified data formats*

Default = '0'
0 - MSB of SDIN data occurs in the first ISCLK period after the ILRCK edge
1 - MSB of SDIN data occurs in the second ISCLK period after the ILRCK edge

SISPOL *- ISCLK clock polarity*

Default = '0'
0 - SDIN sampled on rising edges of ISCLK
1 - SDIN sampled on falling edges of ISCLK

SILRPOL *- ILRCK clock polarity*

Default = '0'
0 - SDIN data is for the left channel when ILRCK is high
1 - SDIN data is for the right channel when ILRCK is high

7.6 Serial Audio Output Port Data Format (6)

7	6	5	4	3	2	1	0
SOMS	SOSF	SORES1	SORES0	SOJUST	SODEL	SOSPOL	SOLRPOL

SOMS *- Master/Slave Mode Selector*

Default = '0'

0 - Serial audio output port is in slave mode

1 - Serial audio output port is in master mode

SOSF *- OSCLK frequency (for master mode)*

Default = '0'

0 - 64*Fso

1 - 128*Fso

SORES1:0 *- Resolution of the output data on SDOUT and on the AES3 output*

Default = '00'

00 - 24 bit resolution

01 - 20 bit resolution

10 - 16 bit resolution

11 - Direct copy of the received NRZ data from the AES3 receiver (including C, U, V and P bits, SDOUT pin only, serial audio output port clock must be derived from the AES3 receiver recovered clock)

SOJUST *- Justification of SDOUT data relative to OLRCK*

Default = '0'

0 - Left-justified

1 - Right-justified (master mode only)

SODEL *- Delay of SDOUT data relative to OLRCK, for left-justified data formats*

Default = '0'

0 - MSB of SDOUT data occurs in the first OSCLK period after the OLRCK edge

1 - MSB of SDOUT data occurs in the second OSCLK period after the OLRCK edge

SOSPOL *- OSCLK clock polarity*

Default = '0'

0 - SDOUT transitions occur on falling edges of OSCLK

1 - SDOUT transitions occur on rising edges of OSCLK

SOLRPOL *- OLRCK clock polarity*

Default = '0'

0 - SDOUT data is for the left channel when OLRCK is high

1 - SDOUT data is for the right channel when OLRCK is high

7.7 Interrupt 1 Status (7) (Read Only)

7	6	5	4	3	2	1	0
TSLIP	OSLIP	0	0	0	DETC	EFTC	RERR

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A ”0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be “0” in this register. This register defaults to 00h.

TSLIP *- AES3 transmitter source data slip interrupt*

In data flows where OMCK, which clocks the AES3 transmitter, is asynchronous to the data source, this bit will go high every time a data sample is dropped or repeated. When TCBL is an input, this bit will go high on receipt of a new TCBL signal.

OSLIP *- Serial audio output port data slip interrupt*

When the serial audio output port is in slave mode, and OLRCK is asynchronous to the port data source, this bit will go high every time a data sample is dropped or repeated.

DETC *- D to E C-buffer transfer interrupt.*

The source for this bit is true during the D to E buffer transfer in the C bit buffer management process.

EFTC *- E to F C-buffer transfer interrupt.*

The source for this bit is true during the E to F buffer transfer in the C bit buffer management process.

RERR *- A receiver error has occurred.*

The Receiver Error register may be read to determine the nature of the error which caused the interrupt.

7.8 Interrupt 2 Status (8) (Read Only)

7	6	5	4	3	2	1	0
0	0	0	0	DETU	EFTU	QCH	0

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A ”0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be “0” in this register. This register defaults to 00h.

DETU *- D to E U-buffer transfer interrupt. (Block Mode only)*

The source of this bit is true during the D to E buffer transfer in the U bit buffer management process.

EFTU *- E to F U-buffer transfer interrupt. (Block Mode only)*

The source of this bit is true during the E to F buffer transfer in the U bit buffer management process.

QCH *- A new block of Q-subcode data is available for reading.*

The data must be completely read within 588 AES3 frames after the interrupt occurs to avoid corruption of the data by the next block.

7.9 Interrupt 1 Mask (9)

7	6	5	4	3	2	1	0
TSLIPM	OSLIPM	0	0	0	DETCM	EFTCM	RERRM

The bits of this register serve as a mask for the Interrupt 1 register. If a mask bit is set to 1, the error is considered unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is considered masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in the Interrupt 1 register. This register defaults to 00h.

7.10 Interrupt 1 Mode MSB (10) & Interrupt 1 Mode LSB (11)

7	6	5	4	3	2	1	0
TSLIP1	OSLIP1	0	0	0	DETC1	EFTC1	RERR1
TSLIP0	OSLIP0	0	0	0	DETC0	EFTC0	RERR0

The two Interrupt 1 Mode registers form a two bit code for each Interrupt 1 function. This code determines whether the INT pin is set active on the arrival of the interrupt condition, on the removal of the interrupt condition, or on the continuing occurrence of the interrupt condition. These registers default to 00h.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

7.11 Interrupt 2 Mask (12)

7	6	5	4	3	2	1	0
0	0	0	0	DETUM	EFTUM	QCHM	0

The bits of this register serve as a mask for the Interrupt 2 register. If a mask bit is set to 1, the error is considered unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is considered masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in the Interrupt 2 register. This register defaults to 00h.

7.12 Interrupt 2 Mode MSB (13) & Interrupt 2 Mode LSB (14)

7	6	5	4	3	2	1	0
0	0	0	0	DETU1	EFTU1	QCH1	0
0	0	0	0	DETU0	EFTU0	QCH0	0

The two Interrupt 2 Mode registers form a two bit code for each Interrupt 2 register function. This code determines whether the INT pin is set active on the arrival of the interrupt condition, on the removal of the interrupt condition, or on the continuing occurrence of the interrupt condition. These registers default to 00h.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

7.13 Receiver Channel Status (15) (Read Only)

7	6	5	4	3	2	1	0
AUX3	AUX2	AUX1	AUX0	PRO	AUDIO	COPY	ORIG

The bits in this register can be associated with either channel A or B of the received data. The desired channel is selected with the CHS bit of the Channel Status Data Buffer Control Register.

AUX3:0 *- Incoming auxiliary data field width, as indicated by the incoming channel status bits, decoded according to IEC60958 and AES3.*

0000 - Auxiliary data is not present
0001 - Auxiliary data is 1 bit long
0010 - Auxiliary data is 2 bits long
0011 - Auxiliary data is 3 bits long
0100 - Auxiliary data is 4 bits long
0101 - Auxiliary data is 5 bits long
0110 - Auxiliary data is 6 bits long
0111 - Auxiliary data is 7 bits long
1000 - Auxiliary data is 8 bits long
1001 - 1111 Reserved

PRO *- Channel status block format indicator*

0 - Received channel status block is in consumer format
1 - Received channel status block is in professional format

$\overline{\text{AUDIO}}$ *- Audio indicator*

0 - Received data is linearly coded PCM audio
1 - Received data is not linearly coded PCM audio

COPY *- SCMS copyright indicator*

0 - Copyright asserted
1 - Copyright not asserted

ORIG *- SCMS generation indicator, decoded from the category code and the L bit.*

0 - Received data is 1st generation or higher
1 - Received data is original

Note: COPY and ORIG will both be set to 1 if the incoming data is flagged as professional, or if the receiver is not in use.

7.14 Receiver Error (16) (Read Only)

7	6	5	4	3	2	1	0
0	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR

This register contains the AES3 receiver and PLL status bits. Unmasked bits will go high on occurrence of the error, and will stay high until the register is read. Reading the register resets all bits to 0, unless the error source is still true. Bits that are masked off in the receiver error mask register will always be 0 in this register.

QCRC - *Q-subcode data CRC error indicator. Updated on Q-subcode block boundaries*

0 - No error

1 - Error

CCRC *- Channel Status Block Cyclic Redundancy Check bit. Updated on CS block boundaries, valid in Pro mode.*

0 - No error

1 - Error

UNLOCK *- PLL lock status bit. Updated on CS block boundaries.*

0 - PLL locked

1 - PLL out of lock

V *- Received AES3 Validity bit status. Updated on sub-frame boundaries.*

0 - Data is valid and is normally linear coded PCM audio

1 - Data is invalid, or may be valid compressed audio

CONF *- Confidence bit. Updated on sub-frame boundaries.*

0 - No error

1 - Confidence error. This indicates that the received data eye opening is less than half a bit period, indicating a poor link that is not meeting specifications.

BIP *- Bi-phase error bit. Updated on sub-frame boundaries.*

0 - No error

1 - Bi-phase error. This indicates an error in the received bi-phase coding.

PAR *- Parity bit. Updated on sub-frame boundaries.*

0 - No error

1 - Parity error

7.15 Receiver Error Mask (17)

7	6	5	4	3	2	1	0
0	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM

The bits in this register serve as masks for the corresponding bits of the Receiver Error register. If a mask bit is set to 1, the error is considered unmasked, meaning that its occurrence will appear in the receiver error register, will affect the RERR pin, will affect the RERR interrupt, and will affect the current audio sample according to the status of the HOLD bit. If a mask bit is set to 0, the error is considered masked, meaning that its occurrence will not appear in the receiver error register, will not affect the RERR pin, will not affect the RERR interrupt, and will not affect the current audio sample. The CCRC and QCRC bits behave differently from the other bits: they do not affect the current audio sample even when unmasked. This register defaults to 00h.

7.16 Channel Status Data Buffer Control (18)

7	6	5	4	3	2	1	0
0	0	BSEL	CBMR	DETCI	EFTCI	CAM	CHS

BSEL *- Selects the data buffer register addresses to contain User data or Channel Status data*

Default = '0'

0 - Data buffer address space contains Channel Status data

1 - Data buffer address space contains User data

CBMR *- Control for the first 5 bytes of channel status "E" buffer*

Default = '0'

0 - Allow D to E buffer transfers to overwrite the first 5 bytes of channel status data

1 - Prevent D to E buffer transfers from overwriting first 5 bytes of channel status data

DETCI *- D to E C-data buffer transfer inhibit bit.*

Default = '0'

0 - Allow C-data D to E buffer transfers

1 - Inhibit C-data D to E buffer transfers

EFTCI *- E to F C-data buffer transfer inhibit bit.*

Default = '0'

0 - Allow C-data E to F buffer transfers

1 - Inhibit C-data E to F buffer transfers

CAM *- C-data buffer control port access mode bit*

Default = '0'

0 - One byte mode

1 - Two byte mode

CHS *- Channel select bit*

Default = '0'

0 - Channel A information is displayed at the $\overline{\text{EMPH}}$ pin and in the receiver channel status register. Channel A information is output during control port reads when CAM is set to 0 (One Byte Mode)

1 - Channel B information is displayed at $\overline{\text{EMPH}}$ pin and in the receiver channel status register. Channel B information is output during control port reads when CAM is set to 0 (One Byte Mode)

7.17 User Data Buffer Control (19)

7	6	5	4	3	2	1	0
0	0	0	UD	UBM1	UBM0	DETUI	EFTUI

UD *- User data pin (U) direction specifier*

Default = '0'

0 - The U pin is an input. The U data is latched in on both rising and falling edges of OLRCK. This setting also chooses the U pin as the source for transmitted U data.

1 - The U pin is an output. The received U data is clocked out on both rising and falling edges of ILRCK. This setting also chooses the U data buffer as the source of transmitted U data.

UBM1:0 *- Sets the operating mode of the AES3 U bit manager*

Default = '00'

00 - Transmit all zeros mode

01 - Block mode

10 - Reserved

11 - Reserved

DETUI *- D to E U-data buffer transfer inhibit bit (valid in block mode only).*

Default = '0'

0 - Allow U-data D to E buffer transfers

1 - Inhibit U-data D to E buffer transfers

EFTUI *- E to F U-data buffer transfer inhibit bit (valid in block mode only).*

Default = '0'

0 - Allow U-data E to F buffer transfers

1 - Inhibit U-data E to F buffer transfer

7.18 Q-Channel Subcode Bytes 0 to 9 (20 - 29) (Read Only)

The following 10 registers contain the decoded Q-channel subcode data

7	6	5	4	3	2	1	0
ADDRESS	ADDRESS	ADDRESS	ADDRESS	CONTROL	CONTROL	CONTROL	CONTROL
TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK
INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX
MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE
SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND
FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME
ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE
ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND
ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME

7.19 OMCK/RMCK Ratio (30) (Read Only)

7	6	5	4	3	2	1	0
ORR7	ORR6	ORR5	ORR4	ORR3	ORR2	ORR1	ORR0

The contents of this register represent the ratio of the OMCK signal to the RMCK signal. The value is represented as an integer and a fractional part.

ORR7:6 *- Integer part of the OMCK/RMCK ratio*

ORR5:0 *- Fractional part of the OMCK/RMCK ratio*

7.20 C-bit or U-bit Data Buffer (32 - 55)

Either channel status data buffer E or user data buffer E (provided UBM bits are set to block mode) is accessible via these register addresses.

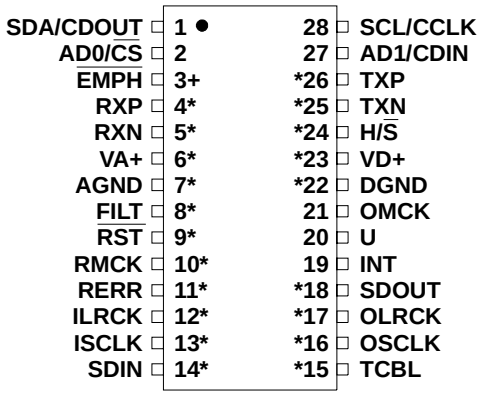
7.21 CS8427 I.D. and Version Register (127) (Read Only)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

ID3:0 *- ID code for the CS8427. Permanently set to 0111*

VER3:0 *- CS8427 revision level. Revision A is coded as 0001*

8. PIN DESCRIPTION - SOFTWARE MODE



* Pins which remain the same function in all modes.
\+ Pins which require a pull up or pull down resistor to select the desired startup option.

SDA/CDOUT	1	**Serial Control Data I/O (I2C) / Data Out (SPI)** (*Input/Output*) - In I^2C mode, SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VD+. In SPI mode, CDOUT is the output data from the control port interface on the CS8427
AD0/$\overline{CS}$	2	**Address Bit 0 (I2C) / Control Port Chip Select (SPI)** (*Input/Output)* - A falling edge on this pin puts the CS8427 into SPI control port mode. With no falling edge, the CS8427 defaults to I^2C mode. In I^2C mode, AD0 is a chip address pin. In SPI mode, $\overline{CS}$ is used to enable the control port interface on the CS8427
$\overline{EMPH}$	3	**Pre-Emphasis** (*Output*) - $\overline{EMPH}$ is low when the incoming AES3 data indicates the presence of 50/15 ms pre-emphasis. When the AES3 data indicates the absence of pre-emphasis or the presence of other than 50/15 ms pre-emphasis $\overline{EMPH}$ is high. This is also a start-up option pin, and requires a 47kΩ resistor to either VD+ or DGND, which determines the AD2 address bit for the control port in I^2C mode
RXP0 **RXN0**	4 5	**Differential Line Receiver** (*Input*) - Receives differential AES3 data.
VA+	6	**Positive Analog Power** (*Input*) - Positive supply for the analog section. Nominally +5V. This supply should be as quiet as possible since noise on this pin will directly affect the jitter performance of the recovered clock
AGND	7	**Analog Ground** (*Input*) - Ground for the analog section. AGND should be connected to the same ground as DGND
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground. Recommended schematic and component values are given in Figure 5 and Tables 1 & 2, respectively. Application note AN159 provides additional resources for the PLL.
$\overline{RST}$	9	**Reset** (*Output*) - When $\overline{RST}$ is low, the CS8427 enters a low power mode and all internal states are reset. On initial power up, $\overline{RST}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase. This is particularly true in hardware mode with multiple CS8427 devices where synchronization between devices is important
RMCK	10	**Input Section Recovered Master Clock** (*Input*/*Output*) - Input section recovered master clock output when PLL is used. Frequency defaults to 256x the sample rate (Fs) and may be set to 128x. When PLL is bypassed via RXD0 bit in Clock Source Control register, an external clock of 256Fs may be applied to this pin

RERR	11	**Receiver Error** (*Output*) - When high, indicates a problem with the operation of the AES3 receiver. The status of this pin is updated once per sub-frame of incoming AES3 data. Conditions that can cause RERR to go high are: validity, parity error, bi-phase coding error, confidence, QCRC and CCRC errors, as well as loss of lock in the PLL. Each condition may be optionally masked from affecting the RERR pin using the Receiver Error Mask Register. The RERR pin tracks the status of the unmasked errors: the pin goes high as soon as an unmasked error occurs and goes low immediately when all unmasked errors go away.
ILRCK	12	**Serial Audio Input Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDIN pin.
ISCLK	13	**Serial Audio Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDIN pin.
SDIN	14	**Serial Audio Data Port** (*Input*) - Audio data serial input pin.
TCBL	15	**Transmit Channel Status Block Start** (*Input*/*Output*) - When operated as output, TCBL is high during the first sub-frame of a transmitted channel status block, and low at all other times. When operated as input, driving TCBL high for at least three OMCK clocks will cause the next transmitted sub-frame to be the start of a channel status block.
OSCLK	16	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	17	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	18	**Serial Audio Output Data** (*Output*) - Audio data serial output pin
INT	19	**Interrupt** (*Output*) -Indicates errors and key events during the operation of the CS8427. All bits affecting INT may be unmasked through bits in the control registers. The condition(s) that initiated interrupt are readable through a control register. The polarity of the INT output, as well as selection of a standard or open drain output, is set via a control register. Once set true, the INT pin goes false only after the interrupt status registers have been read and the interrupt status bits have returned to zero
U	20	**User Data** (*Output*) - May optionally be used to input User data for transmission by the AES3 transmitter, see Figure 15 for timing information. Alternatively, the U pin may be set to output User data from the AES3 receiver, see Figure 15 for timing information. If not driven, a 47kΩ pull-down resistor is recommended for the U pin, since the default state of the UD direction bit sets the U pin as an input. The pull-down resistor ensures that the transmitted user data will be zero. If the U pin is always set to be an output, thereby causing the U bit manager to be the source of the U data, then the resistor is not necessary. The U pin should not be tied directly to ground, in case it is programmed to be an output, and subsequently tries to output a logic high. This situation may affect the long term reliability of the device. If the U pin is driven by a logic level output, then a 100 Ω series resistor is recommended.
OMCK	21	**System Clock** (*Input*) - When the OMCK System Clock Mode is enabled by the SWCLK bit in the Control 1 register, the clock signal input on this pin is output through RMCK. OMCK serves as reference signal for OMCK/RMCK ratio expressed in register 30
DGND	22	**Digital Ground** (*Input*) - Ground for the digital section. DGND should be connected to the same ground as AGND
VD+	23	**Positive Digital Power** (*Input*) - Typically +3 to +5V.
H/$\overline{S}$	24	**Hardware/Software Mode Control** (*Input*) - Determines the method of controlling the operation of the CS8427, and the method of accessing CS and U data. In software mode, device control and CS and U data access is primarily via the control port, using a microcontroller. Hardware mode provides an alternate mode of operation and access to the CS and U data via dedicated pins. This pin should be permanently tied to VD+ or DGND
TXN **TXN**	25 26	**Differential Line Driver** (*Output*) - Drivers transmit AES3 data and are pulled low while the CS8427 is in the reset state.
AD1/CDIN	27	**Address Bit 1 (I2C) / Serial Control Data in (SPI)** (*Input*) - In I^2C mode, AD1 is a chip address pin. In SPI mode, CDIN is the input data line for the control port interface
SCL/CCLK	28	**Control Port Clock** (*Input*) - Serial control interface clock and is used to clock control data bits into and out of the CS8427. In I^2C mode, SCL requires an external pull-up resistor to VD+

9. HARDWARE MODE DESCRIPTION

Hardware mode is selected by connecting the H/$\overline{S}$ pin to '1'. Hardware Mode data flow is shown in Figure 21. Audio data is input via the AES3 receiver, and routed to the serial audio output port. Different audio data synchronous to RMCK may be input into the serial audio input port, and output via the AES3 transmitter.

The channel status data, user data and validity bit information are handled in 2 alternative modes: A and B, determined by a start-up resistor on the COPY pin. In mode A, the received PRO, COPY, ORIG, $\overline{\text{EMPH}}$, and $\overline{\text{AUDIO}}$ channel status bits are output on pins. The transmitted channel status bits are copied from the received channel status data, and the transmitted U and V bits are 0.

In mode B, only the COPY and ORIG pins are output, and reflect the received channel status data. The transmitted channel status bits, user data and validity bits are input serially via the PRO/C, $\overline{\text{EMPH}}$/U and $\overline{\text{AUDIO}}$/V pins. Figure 15 shows the timing requirements.

The APMS pin allows the serial audio input port to be set to master or slave.

If a validity, parity, bi-phase or lock receiver error occurs, the current audio sample is passed unmodified to the serial audio output port.

Start-up options are shown in Table 4, and allow choice of the serial audio output port as a master or slave, whether TCBL is an input or an output, the audio serial ports formats and the source of the transmitted C, U and V data.

9.1 Serial Audio Port Formats

In hardware mode, only a limited number of alternative serial audio port formats are available. These formats are described by Tables 5 & 6, which define the equivalent software mode bit settings for each format. Timing diagrams are shown in Figures 17 and 18.

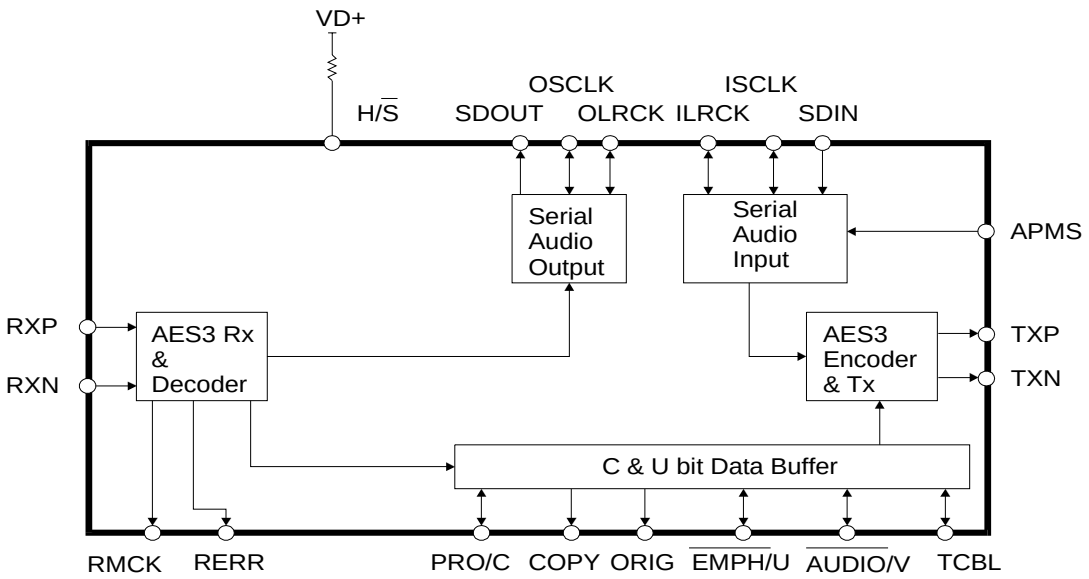


Figure 21. Hardware Mode

SDOUT	RMCK	RERR	ORIG	COPY	Function
LO	-	-	-	-	Serial Output Port is Slave
HI	-	-	-	-	Serial Output Port is Master
-	-	-	-	LO	Mode A: C transmitted data is copied from received data, U and V =0, received PRO, EMPH, AUDIO is visible
-	-	-	-	HI	Mode B: CUV transmitted data is input serially on pins, received PRO, EMPH and AUDIO is not visible
-	LO	LO	-	-	Serial Input & Output Format IF1&OF1
-	LO	HI	-	-	Serial Input & Output Format IF2&OF2
-	HI	LO	-	-	Serial Input & Output Format IF3&OF3
-	HI	HI	-	-	Serial Input & Output Format IF1&OF5
-	-	-	LO	-	TCBL is an input
-	-	-	HI	-	TCBL is an output

Table 4. Hardware Mode Start-up Options

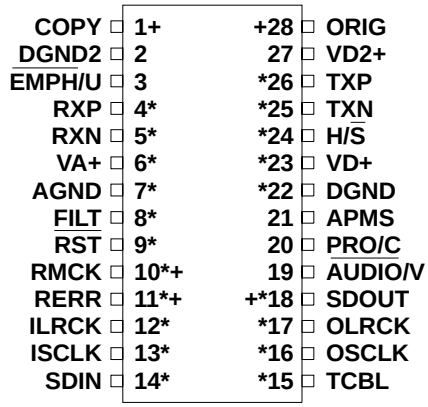
	SOSF	SORES1/0	SOJUST	SODEL	SOSPOL	SOLRPOL
OF1 - Left Justified	0	00	0	0	0	0
OF2 - I^2S 24-bit data	0	00	0	1	0	1
OF3 - Right Justified, master mode only	0	00	1	0	0	0
OF4 - I^2S 16 bit data	0	10	0	1	0	1
OF5 - Direct AES3 data	0	11	0	0	0	0

Table 5. Serial Audio Output Formats Available in Hardware Mode

	SISF	SIRES1/0	SIJUST	SIDEL	SISPOL	SILRPOL
IF1 - Left Justified	0	00	0	0	0	0
IF2 - I^2S	0	00	0	1	0	1
IF3 - Right Justified 24-bit data	0	00	1	0	0	0
IF4 - Right Justified 16-bit data	0	10	1	0	0	0

Table 6. Serial Audio Input Formats Available in Hardware Mode

10. PIN DESCRIPTION - HARDWARE MODE



* Pins which remain the same function in all modes.
\+ Pins which require a pull up or pull down resistor to select the desired startup option.

COPY	1	**COPY Channel Status Bit** (*Output*) - Reflects the state of the COPY Channel Status bit in the incoming AES3 data stream. This is also a start-up option pin, and requires a pull-up or pull-down resistor.
DGND2 **DGND**	2 22	**Digital Ground** (*Input*) - Ground for the digital section. DGND should be connected to the same ground as AGND.
EMPH/U	3	**Pre-Emphasis Indicator / U-bit** (*Input*/*Output*) - The EMPH/U pin either reflects the state of the EMPH channel status bit in the incoming AES3 data stream, or is the serial U-bit input for the AES3 transmitted data, clocked by OLRCK. If indicating emphasis, then EMPH/U is low when the incoming data indicates 50/15 µs pre-emphasis, and high otherwise.
RXP0 **RXN0**	4 5	**Differential Line Receiver** (*Input*) - Receives differential AES3 data.
VA+	6	**Positive Analog Power** (*Input*) - Positive supply for the analog section. Nominally +5V. This supply should be as quiet as possible since noise on this pin will directly affect the jitter performance of the recovered clock
AGND	7	**Analog Ground** (*Input*) - Ground for the analog section. AGND should be connected to the same ground as DGND
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground. Recommended schematic and component values are given in Figure 5 and Tables 1 & 2, respectively. Application note AN159 provides additional resources for the PLL.
RST	9	**Reset** (*Output*) - When RST is low, the CS8427 enters a low power mode and all internal states are reset. On initial power up, RST must be held low until the power supply is stable, and all input clocks are stable in frequency and phase. This is particularly true in hardware mode with multiple CS8427 devices where synchronization between devices is important
RMCK	10	**Input Section Recovered Master Clock** (*Input*/*Output*) - Input section recovered master clock output when PLL is used. Frequency is 256x the sample rate (Fs).
RERR	11	**Receiver Error** (*Output*) - When high, indicates a problem with the operation of the AES3 receiver. The status of this pin is updated once per sub-frame of incoming AES3 data. Conditions that can cause RERR to go high are: parity error, bi-phase coding error, confidence, QCRC and CCRC errors, as well as loss of lock in the PLL.
ILRCK	12	**Serial Audio Input Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDIN pin.
ISCLK	13	**Serial Audio Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDIN pin.
SDIN	14	**Serial Audio Data Port** (*Input*) - Audio data serial input pin.

TCBL	15	**Transmit Channel Status Block Start** (*Input*/*Output*) - When operated as output, TCBL is high during the first sub-frame of a transmitted channel status block, and low at all other times. When operated as input, driving TCBL high for at least three OMCK clocks will cause the next transmitted sub-frame to be the start of a channel status block.
OSCLK	16	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	17	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	18	**Serial Audio Output Data** (*Output*) - Audio data serial output pin
$\overline{\text{AUDIO}}$/V	19	**Audio Channel Status Bit / V-Bit** (*Input*/*Output*) - Reflects either the state of the audio/non audio Channel Status bit in the incoming AES3 data stream or is the V-bit data input for the AES3 transmitted data stream, clocked by OLRCK.
PRO/C	20	**PRO Channel Status Bit / C-Bit** (*Input*/*Output*) - Reflects either the state of the Professional/Consumer Channel Status bit in the incoming AES3 data stream or is the serial C-bit input for the AES3 transmitted data, clocked by OLRCK.
APMS	21	**Serial Audio Input Port Master/Slave Select** (*Input*) - APMS should be connected to VD+ to set serial audio input port as a master, or connected to DGND to set the port as a slave.
VD+ **VD2+**	23 27	**Positive Digital Power** (*Input*) - Typically +3 to +5V.
H/$\overline{\text{S}}$	24	**Hardware/Software Mode Control** (*Input*) - Determines the method of controlling the operation of the CS8427, and the method of accessing CS and U data. In software mode, device control and CS and U data access is primarily via the control port, using a microcontroller. Hardware mode provides an alternate mode of operation and access to the CS and U data via dedicated pins. This pin should be permanently tied to VD+ or DGND
TXN **TXN**	25 26	**Differential Line Driver** (*Output*) - Drivers transmit AES3 data and are pulled low while the CS8427 is in the reset state.
ORIG	28	**ORIG Channel Status Bit** (*Output*) - SCMS generation indicator. This is decoded from the incoming category code and the L bit. A low output indicates that the audio data stream is 1st generation or higher. A high indicates that the audio data stream is original. This is also a start-up option pin, and requires a pull-up or pull-down resistor.

11. APPLICATIONS

11.1 Reset, Power Down and Start-up

When $\overline{RST}$ is low, the CS8427 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. When $\overline{RST}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 1 to the RUN bit will then cause the part to leave the low power state and begin operation. After the PLL has settled, the AES3 and serial audio outputs will be enabled.

Some options within the CS8427 are controlled by a start-up mechanism. During the reset state, some of the output pins are reconfigured internally to be inputs. Immediately upon exiting the reset state, the level of these pins is sensed. The pins are then switched to be outputs. This mechanism allows output pins to be used to set alternative modes in the CS8427 by connecting a 47kΩ resistor to between the pin and either VD+ (HI) or DGND (LO). For each mode, every start-up option select pin MUST have an external pull-up or pull-down resistor. In software mode, the only start-up option pin is $\overline{EMPH}$, which is used to set a chip address bit for the control port in I^2C mode. Hardware modes use many start-up options, which are detailed in the hardware definition section at the end of this data sheet.

11.2 ID Code and Revision Code

The CS8427 has a register that contains a four bit code to indicate that the addressed device is a CS8427. This is useful when other CS84XX family members are resident in the same system, allowing common software modules.

The CS8427 four bit revision code is also available. This allows the software driver for the CS8427 to identify which revision of the device is in a particular system, and modify its behavior accordingly. To allow for future revisions, it is strongly recommend that the revision code is read into a variable area within the microcontroller, and used wherever appropriate as revision details become known.

11.3 Power Supply, Grounding, and PCB layout

For most applications, the CS8427 can be operated from a single +5V supply, following normal supply decoupling practices, see Figure 5. For applications where the recovered input clock, output on the RMCK pin, is required to be low jitter, then use a separate, quiet, analog +5V supply for VA+, decoupled to AGND. In addition, a separate region of analog ground plane around the FILT, AGND, VA+, RXP and RXN pins is recommended.

The VD+ supply should be well decoupled with a 0.1µF capacitor to DGND to minimize AES3 transmitter induced transients.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the CS8427 to minimize inductance effects, and all decoupling capacitors should be as close to the CS8427 as possible.

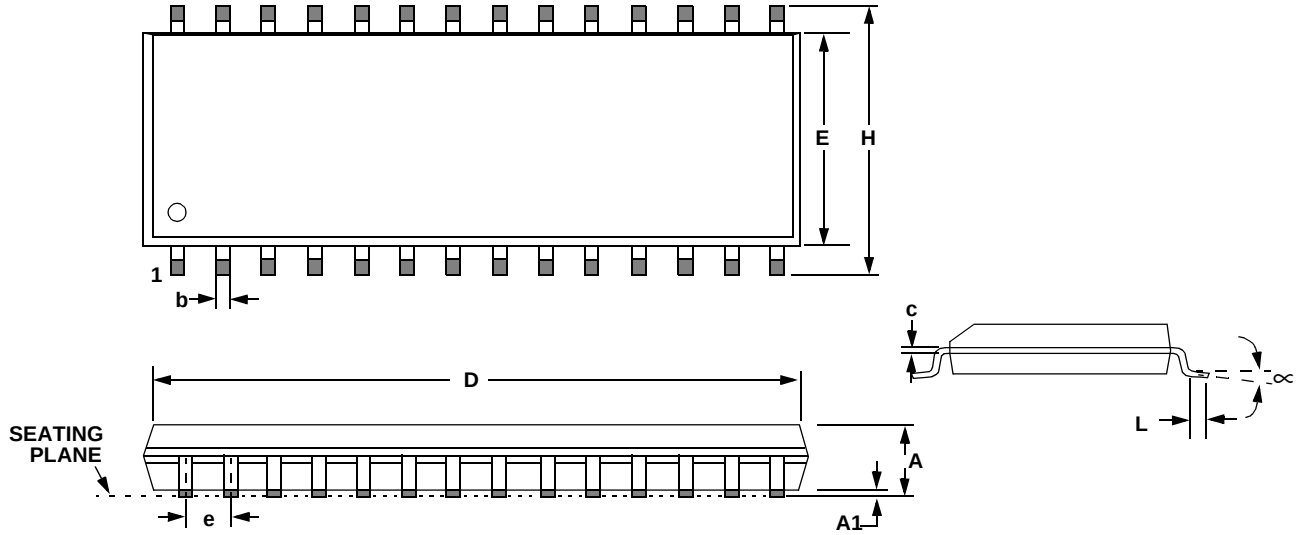
11.4 Synchronization of Multiple CS8427s

The serial audio output ports of multiple CS8427s can be synchronized if all devices share the same master clock, OSCLK, OLRCK, and $\overline{\text{RST}}$ line and leave the reset state on the same master clock falling edge. Either all the ports need to be in slave mode, or one can be set as a master.

Multiple AES3 transmitters can be synchronized if all devices share the same master clock, TCBL, and $\overline{\text{RST}}$ signals and leave the reset state on the same master clock falling edge. The TCBL pin is used to synchronize multiple CS8427 AES3 transmitters at the channel status block boundaries. One CS8427 must have its TCBL set to master; the others must be set to slave TCBL. Alternatively, TCBL can be derived from external logic, in which case all the CS8427 devices should be set to slave TCBL.

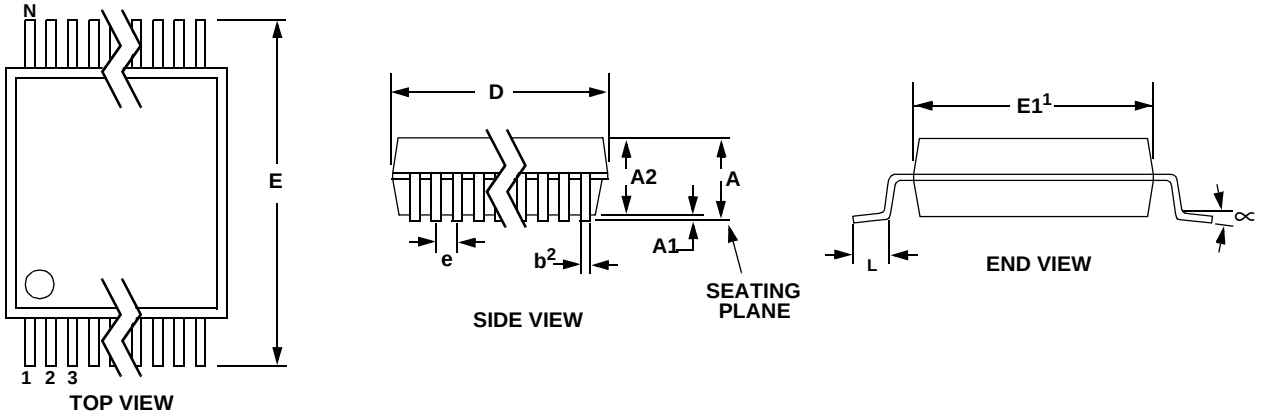
12. PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

28L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	**--**	**--**	**0.47**	**--**	**--**	**1.20**	
A1	**0.002**	**0.004**	**0.006**	**0.05**	**--**	**0.15**	
A2	**0.03150**	**0.03937**	**0.0413**	**0.80**	**1.00**	**1.05**	
b	**0.00748**	**0.0096**	**0.012**	**0.19**	**0.245**	**0.30**	2,3
D	**0.378 BSC**	**0.382 BSC**	**0.386 BSC**	**9.60 BSC**	**9.70 BSC**	**9.80 BSC**	1
E	**0.248**	**0.2519**	**0.256**	**6.30**	**6.40**	**6.50**	
E1	**0.169**	**0.1732**	**0.177**	**4.30**	**4.40**	**4.50**	1
e	**--**	**0.026 BSC**	**--**	**--**	**0.65 BSC**	**--**	
L	**0.020**	**0.024**	**0.029**	**0.50**	**0.60**	**0.75**	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

13. APPENDIX A: EXTERNAL AES3/SPDIF/IEC60958 TRANSMITTER AND RECEIVER COMPONENTS

This section details the external components required to interface the AES3 transmitter and receiver to cables and fiber-optic components.

13.1 AES3 Transmitter External Components

The output drivers on the CS8427 are designed to drive both the professional and consumer interfaces. The AES3 specification for professional/broadcast use calls for a 110 Ω source impedance and a balanced drive capability. Since the transmitter output impedance is very low, a 110 Ω resistor should be placed in series with one of the transmit pins. The specifications call for a balanced output drive of 2-7 volts peak-to-peak into a 110 Ω load with no cable attached. Using the circuit in Figure 22, the output of the transformer is short-circuit protected, has the proper source impedance, and provides a 5 volt peak-to-peak signal into a 110 Ω load. Lastly, the two output pins should be attached to an XLR connector with male pins and a female shell, and with pin 1 of the connector grounded.

In the case of consumer use, the IEC60958 specifications call for an unbalanced drive circuit with an output impedance of 75 Ω and a output drive level of 0.5 volts peak-to-peak ±20% when measured across a 75 Ω load using no cable. The circuit shown in Figure 23 only uses the TXP pin and provides the proper output impedance and drive level using standard 1% resistors. The connector for a consumer application would be an RCA phono socket. This circuit is also short circuit protected. The TXP pin may be used to drive TTL or CMOS gates as shown in Figure 24. This circuit may be used for optical connectors for digital audio since they usually have TTL or CMOS compatible inputs. This circuit is also useful when driving multiple digital audio outputs since RS422 line drivers have TTL compatible inputs.

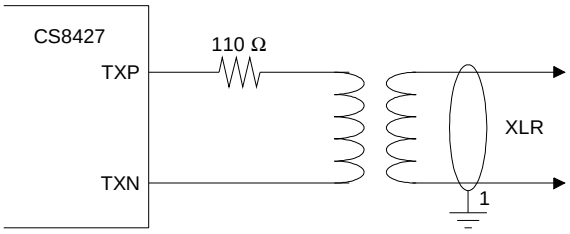


Figure 22. Professional Output Circuit

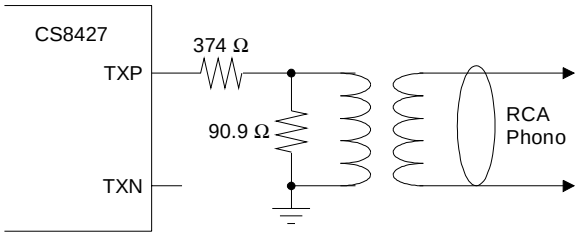


Figure 23. Consumer Output Circuit

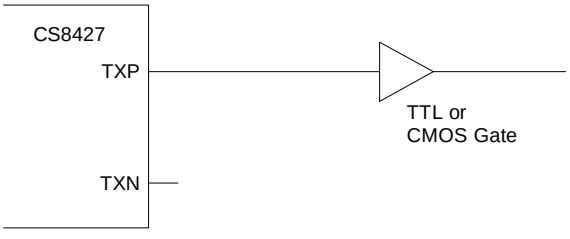


Figure 24. TTL/CMOS Output Circuit

13.2 AES3 Receiver External Components

The CS8427 AES3 receiver is designed to accept both the professional and consumer interfaces. The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110Ω ±20% impedance. The XLR connector on the receiver should have female pins with a male shell. Since the receiver has a very high input impedance, a 110Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in Figure 25. Although transformers are not required by the AES, they are, however, strongly recommended.

If some isolation is desired without the use of transformers, a 0.01µF capacitor should be placed in series with each input pin (RXP and RXN) as shown in Figure 26. However, if a transformer is not used, high frequency energy could be coupled into the receiver, causing degradation in analog performance.

Figures 25 and 26 show an optional DC blocking capacitor (0.1µF to 0.47µF) in series with the cable input. This improves the robustness of the receiver, preventing the saturation of the transformer, or any DC current flow, if a DC voltage is present on the cable.

In the configuration of systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could result when boxes with different ground potentials are connected. Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantageous to have the ground of two boxes held to the same potential, and the cable shield might be depended upon to make that electrical connection. Generally, it may be a good idea to provide the option of grounding or capacitively coupling the shield to the chassis.

In the case of the consumer interface, the standards call for an unbalanced circuit having a receiver impedance of 75 Ω ±5%. The connector for the consumer interface is an RCA phono socket. The receiver circuit for the consumer interface is shown in Figure 27.

The circuit shown in Figure 28 may be used when external RS422 receivers, optical receivers or other TTL/CMOS logic outputs drive the CS8427 receiver section.

13.3 Isolating Transformer Requirements

Please refer to the application note AN134: "AES and SPDIF Recommended Transformers" for resources on transformer selection.

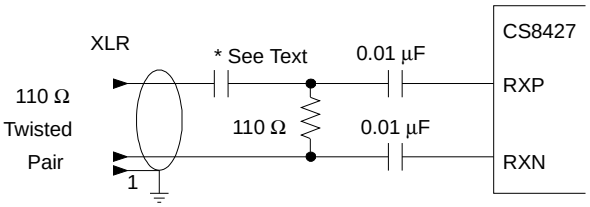


Figure 25. Professional Input Circuit

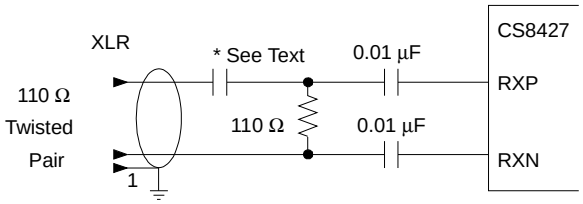


Figure 26. Transformerless Professional Input Circuit

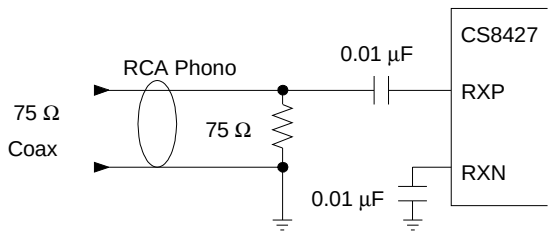


Figure 27. Consumer Input Circuit

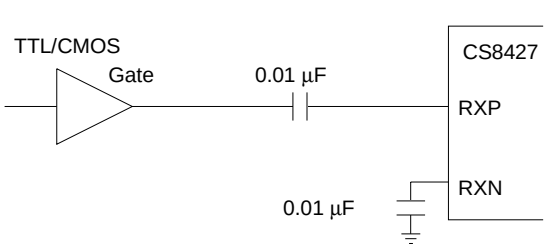


Figure 28. TTL/CMOS Input Circuit

14. APPENDIX B: CHANNEL STATUS AND USER DATA BUFFER MANAGEMENT

The CS8427 has a comprehensive channel status (C) and user (U) data buffering scheme, which allows automatic management of channel status blocks and user data. Alternatively, sufficient control and access is provided to allow the user to completely manage the C and U data via the control port.

14.1 AES3 Channel Status(C) Bit Management

The CS8427 contains sufficient RAM to store a full block of C data for both A and B channels (192x2 = 384 bits), and also 384 bits of U information. The user may read from or write to these RAMs via the control port.

The CS8427 manages the flow of channel status data at the block level, meaning that entire blocks of channel status information are buffered at the input, synchronized to the output timebase, and then transmitted. The buffering scheme involves a cascade of 3 block-sized buffers, named D,E and F, as shown in Figure 29. The MSB of each byte represents the first bit in the serial C data stream. For example, the MSB of byte 0 (which is at control port address 32) is the consumer/professional bit for channel status block A.

The first buffer, D, accepts incoming C data from the AES receiver. The 2nd buffer, E, accepts entire blocks of data from the D buffer. The E buffer is also accessible from the control port, allowing read and writing of the C data. The 3rd buffer (F) is used as the source of C data for the AES3 transmitter. The F buffer accepts block transfers from the E buffer.

14.1.1 Manually accessing the E buffer

The user can monitor the data being transferred by reading the E buffer, which is mapped into the register space of the CS8427, via the control port. The user can modify the data to be transmitted by writing to the E buffer.

The user can configure the interrupt enable register to cause interrupts to occur whenever “D to E” or “E to F” buffer transfers occur. This allows determination of the allowable time periods to interact with the E buffer.

Also provided are “D to E” and “E to F” inhibit bits. The associated buffer transfer is disabled whenever the user sets these bits. These may be used whenever “long” control port interactions are occurring. They can also be used to align the be-

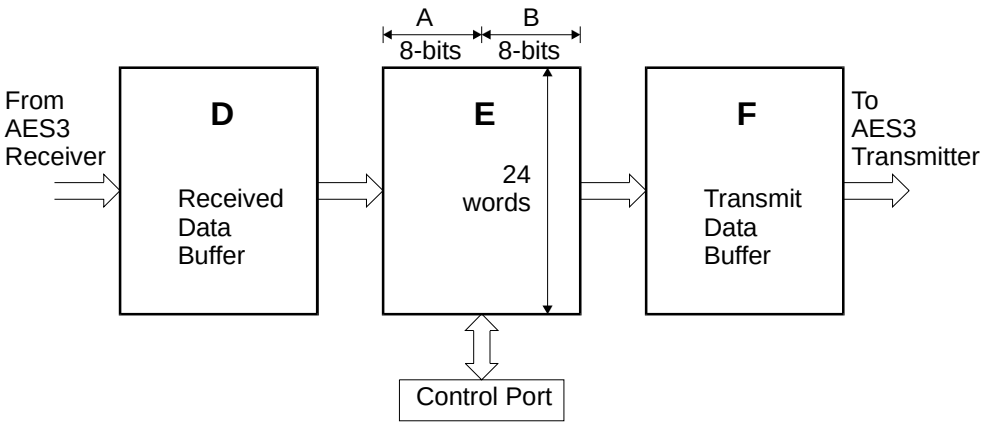


Figure 29. Channel Status Data Buffer Structure

havior of the buffers with the selected audio data flow. For example, if the audio data flow is serial port in to AES3 out, then it is necessary to inhibit "D toE" transfers, since these would overwrite the desired transmit C data with invalid data.

Flowcharts for reading and writing to the E buffer are shown in Figures 30 and 31. For reading, since a D to E interrupt just occurred, then there a substantial time interval until the next D to E transfer (approximately 24 frames worth of time). This is usually plenty of time to access the E data without having to inhibit the next transfer.

For writing, the sequence starts after a E to F transfer, which is based on the output timebase. Since a D to E transfer could occur at any time (this is based on the input timebase), then it is important to inhibit D to E transfers while writing to the E buffer until all writes are complete. Then wait until the next E to F transfer occurs before enabling D to E transfers. This ensures that the data written to the E buffer actually gets transmitted and not overwritten by a D to E transfer.

If the channel status block to transmit indicates PRO mode, then the CRCC byte is automatically calculated by the CS8427, and does not have to be written into the last byte of the block by the host microcontroller.

14.1.2 Reserving the first 5 bytes in the E buffer

D to E buffer transfers periodically overwrite the data stored in the E buffer. This can be a problem for users who want to transmit certain channel status settings which are different from the incoming settings. In this case, the user would have to superimpose his settings on the E buffer after every D to E overwrite.

To avoid this problem, the CS8427 has the capability of reserving the first 5 bytes of the E buffer for user writes only. When this capability is in use, internal D to E buffer transfers will NOT affect the first 5 bytes of the E buffer. Therefore, the user can set values in these first 5 E bytes once, and the settings will persist until the next user change. This mode is enabled via the Channel Status Data Buffer Control register.

14.1.3 Serial Copy Management System (SCMS)

In software mode, the CS8427 allows read/modify/write access to all the channel status bits. For consumer mode SCMS compliance, the host microcontroller needs to read and manipulate the Category Code, Copy bit and L bit appropriately.

In hardware mode, the SCMS protocol can be followed by either using the COPY and ORIG input pins, or by using the C bit serial input pin. These options are documented in the hardware mode section of this data sheet.

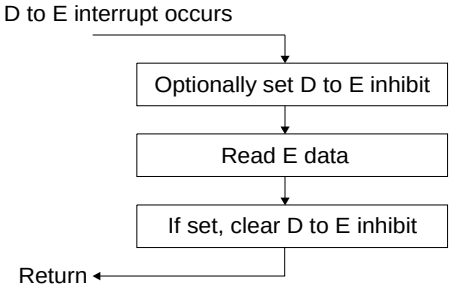


Figure 30. Flowchart for Reading the E Buffer

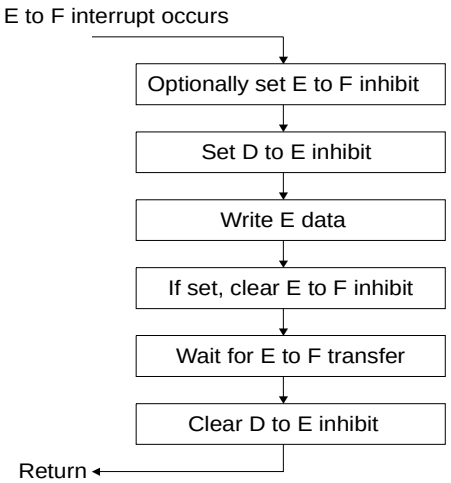


Figure 31. Flowchart for Writing the E Buffer

14.1.4 Channel Status Data E Buffer Access

The E buffer is organized as 24 x 16-bit words. For each word the MS Byte is the A channel data, and the LS Byte is the B channel data (see Figure 29).

There are two methods of accessing this memory, known as one byte mode and two byte mode. The desired mode is selected via a control register bit.

One Byte mode

In many applications, the channel status blocks for the A and B channels will be identical. In this situation, if the user reads a byte from one of the channel's blocks, the corresponding byte for the other channel will be the same. Similarly, if the user wrote a byte to one channel's block, it would be necessary to write the same byte to the other block. One byte mode takes advantage of the often identical nature of A and B channel status data.

When reading data in one byte mode, a single byte is returned, which can be from channel A or B data, depending on a register control bit. If a write is being done, the CS8427 expects a single byte to be input to its control port. This byte will be written to both the A and B locations in the addressed word.

One byte mode saves the user substantial control port access time, as it effectively accesses 2 bytes worth of information in 1 byte's worth of access time. If the control port's autoincrement addressing is used in combination with this mode, multi-byte accesses such as full-block reads or writes can be done especially efficiently.

Two Byte mode

There are those applications in which the A and B channel status blocks will not be the same, and the user is interested in accessing both blocks. In these situations, two byte mode should be used to access the E buffer.

In this mode, a read will cause the CS8427 to output two bytes from its control port. The first byte out will represent the A channel status data, and the 2nd byte will represent the B channel status data. Writing is similar, in that two bytes must now be input to the CS8427's control port. The A channel status data is first, B channel status data second.

14.2 AES3 User (U) Bit Management

The CS8427 U bit manager has two operating modes: transmit all zeros and block mode.

14.2.1 Mode 1: Transmit All Zeros

Mode 1 causes only zeros to be transmitted in the output U data, regardless of E buffer contents or U data embedded in an input AES3 data stream. This mode is intended for the user who does not want to transceive U data, and simply wants the output U channel to contain no data.

14.2.2 Mode 2: Block Mode

Mode 2 is very similar to the scheme used to control the C bits. Entire blocks of U data are buffered from input to output, using a cascade of 3 block-sized RAMs to perform the buffering. The user has access to the second of these 3 buffers, denoted the E buffer, via the control port. Block mode is designed for use in AES3 in, AES3 out situations in which input U data is decoded using a microcontroller via the control port. It is also the only mode in which the user can merge his own U data into the transmitted AES3 data stream.

The U buffer access only operates in two byte mode, since there is no concept of A and B blocks for user data. The arrangement of the data in the each byte is that the MSB is the first received bit and is the first transmitted bit. The first byte read is the first byte received, and the first byte sent is the first byte transmitted.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